MediaPad 10 FHD Maintenance Manual

V1.0

For internal use only

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HUAWEI

Huawei Technologies Co., Ltd.

Change History

Date	Revision Version	Change Reason	Changed Chapter	Change Description	Author
2012-7-14	V1.0				

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1 Product Overview

1.1 Brief Introduction

Background

10-inch tablets take a share of more than 70% of the tablet market. As a mainstream model of tablets, they provide Internet surfing, pleasant visual experience, and portable use. 10-inch tablets have found their way in a variety of application fields, such as retailing, operators' mobile broadband product reselling, operators' promotion of new home products, enterprise office administration, and financial insurance.

MediaPad 10 FHD is a 10-inch tablet of Huawei MediaPad series based on the Android 4.0 (Ice Cream Sandwich) operating system. Its hardware integrates an access point (AP) and a modem (K3+BalongV7). Equipped with a 10.1-inch in-plane switching (IPS) thin-film transistor (TFT) LCD, the MediaPad 10 FHD features high resolution (1920 x 1200 pixels) and provides complete touchscreen operations. It supports multiple audio and video formats, such as MP3, MP4, AVI, ASF, and WAV.

The MediaPad 10 FHD also provides the following auxiliary functions:

- 8.0 megapixel (MP) camera
- microSD card
- Global positioning system (GPS)
- Wireless Fidelity (Wi-Fi)
- Bluetooth 4.0
- Frequency modulation (FM)
- Acceleration sensor
- Proximity sensor
- Light sensor
- Gyroscope sensor
- Compass
- Electromagnetic sensor

In terms of wireless communication, the MediaPad 10 FHD supports the following features:

- GSM mode: GPRS and EDGE
- WCDMA mode: UMTS, HSDPA, and HSPA+
- WCDMA frequency bands: bands 1, 2, 5, 8, 9, and 11
- GSM frequency bands: 850 MHz, 900 MHz, 1800 MHz, and 1900 MHz.

The entire device has five antennas: one host antenna, one diversity antenna, one GPS antenna, one antenna for the Bluetooth and Wi-Fi modules, and one independent antenna for the synthetic aperture radar (SAR) sensor.

The smart chip MAX8903 is used for charging management, the Broadcom BCM4330 chip is used for the Wi-Fi and Bluetooth modules, and the BCM47511 chip is used for the GPS module.

The MediaPad 10 FHD has the following memory features:

- AP RAM: LP DDR2, standard 1 GB 533 Hz (compatible with 2 GB)
- AP ROM: eMMC, standard 8 GB (compatible with 16 GB and 32 GB)
- Modem: Hi6920+Hi6451+Hi6360, MCP (NAND+DDR), standard 2 Gbit + 1 Gbit (compatible with 1 Gbit + 512 Mbit)

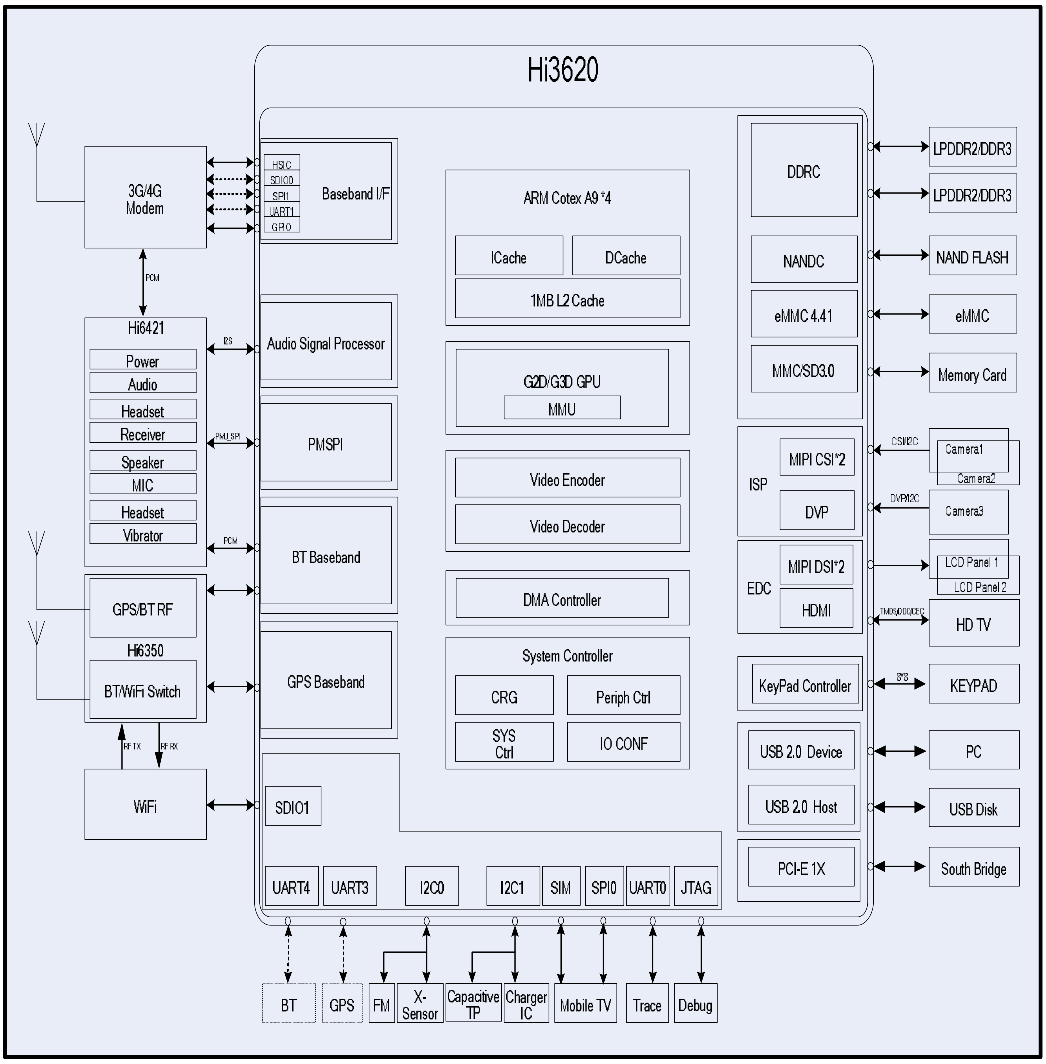
The MediaPad 10 FHD supports the 3.5 mm headset jack and 30-pin dock interface. The dock interface supports multiple functions, such as charging, power supply, USB host or device installation, and the display port.

Figure 1-1 shows the appearance of the MediaPad 10 FHD.

Figure 1-1 Appearance of the MediaPad 10 FHD

Figure 1-2 shows the hardware principles of the MediaPad 10 FHD (Hi3620+Hi6920).

Figure 1-2 Hardware principles of the MediaPad 10 FHD



Board Functions

The main control board provides the following functions:

- Provides the host CPU and processes image signals.
- Manages host power supply.
- Supports UMTS (WCDMA), HSPA, GSM, GPRS, and EDGE.
- Supports GPS.
- Provides LCD and camera interfaces.
- Provides audio interfaces.
- Provides a WLAN or Bluetooth module.

The interface board provides the following functions:

- Provides dock interfaces.
- Provides USB and charging interfaces.

Table 1-1 lists the hardware interfaces provided by the MediaPad 10 FHD.

Table 1-1 External hardware interfaces

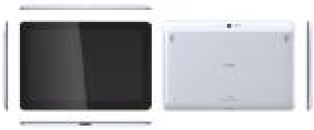
No.	Interface Type	Physical Interface Mode	Number of Interfaces	Remarks
1	USB	OTG	1	This interface is used to connect to a PC or other devices. It complies with the USB 2.0 specification.
2	3G	Main antenna and diversity antenna	2	This interface is an uplink data interface for voice services (WCDMA).
3	WLAN	Built-in antenna	1	This interface is used to connect to a local WLAN device.
4	Dock interface	Dock jack	1	This interface provides numerous communication signals, such as power input, MHL, and USB signals.
5	Power switch	Tact switch	1	Power switch
6	Key	Sound volume adjustment key	2	VOL+, VOL-
7	Touchscreen	Capacitor screen, I2C interface	1	Compatible with the resistor-capacitor
8	LCD	MIPI	1	1920 x 1080 pixels
9	JTAG interface	Normalized 9-pin encapsulation	1	This JTAG interface is used for program loading.
10				
11				
12				
13				

1.2 Hardware Specifications

Table 1-2 lists the hardware specifications of the MediaPad 10 FHD.

Table 1-2 Hardware specifications of the MediaPad 10 FHD

Technical Parameter	Specification
Dimensions (H x W x D)	8.9 mm x 267.2 mm x 169.8 mm
Weight	About 630 g (TBD)

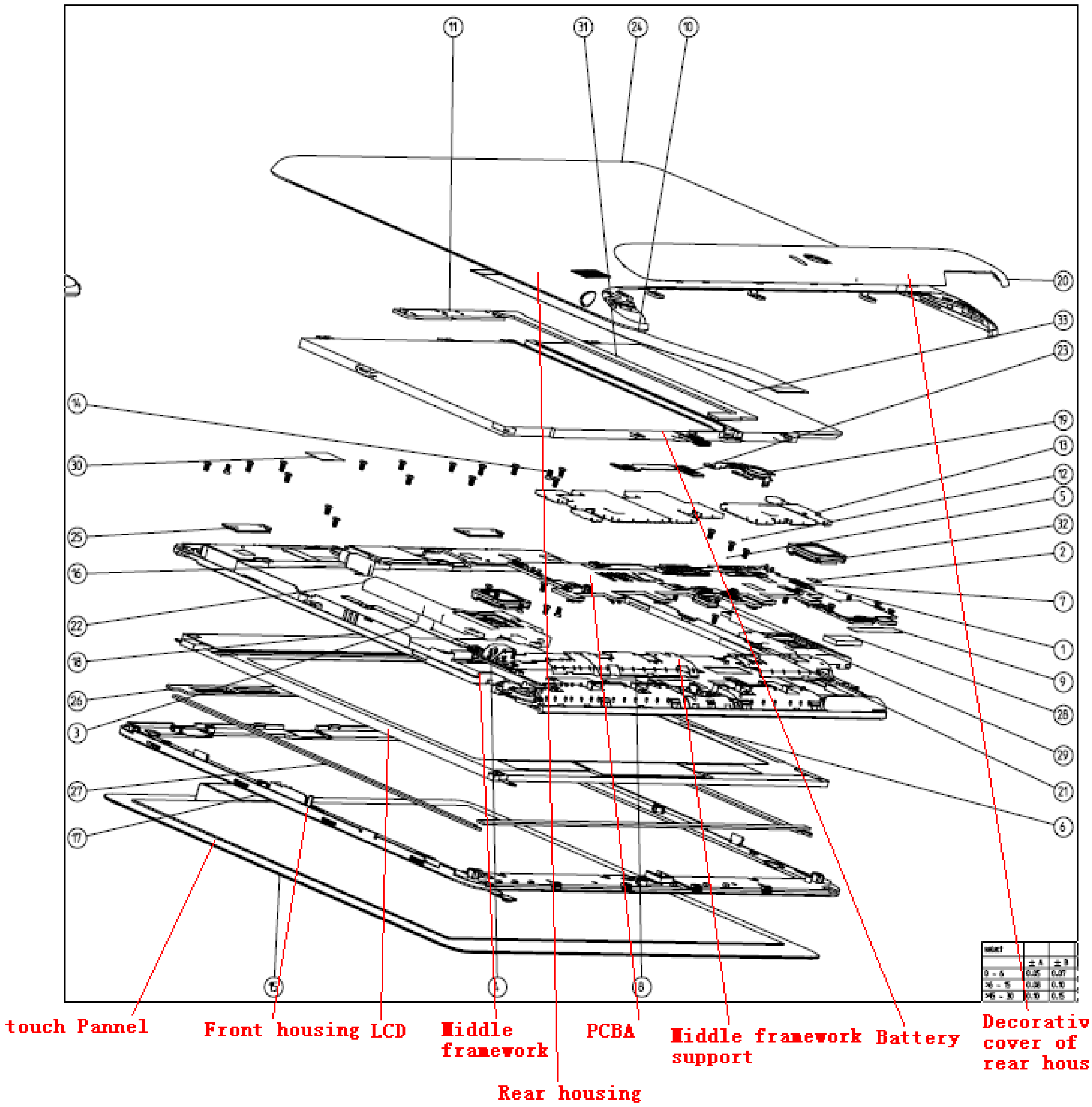
Technical Parameter	Specification
Shape	
Battery	6300 mA
Display	10.1-inch WXGA (1920 x 1200 pixels), TFT, touchscreen
Touch panel	Capacitive, Multi-touch (10 points)
Interface	30-pin dock connector 3.5 mm headset jack
Band	S10-101u: UMTS 2100/900, EDGE/GPRS/GSM (850/900/1800/1900) S10-102u: UMTS 2100/1900/850, EDGE/GPRS/GSM (850/900/1800/1900)
	HSPA+: 42 Mbit/s
Chipset	Hi3620T (K3 V2) + Hi6920 (Balong V7)
OS	Android 4.0 (Ice Cream Sandwich)
Memory	RAM: 2 GB ROM: 16 GB Maximum 32 GB microSD card
Multimedia	Rear camera: 8.0 MP HD AF, dual LED flash Front camera: 1.3 MP HD H.263, MPEG4, H.264 (decode) MP3, AAC, AAC+
Network service	3G
Others	Wi-Fi b/g/n, Bluetooth v3.0 +HS, DLNA, 30-pin dock connector, 1080p video

1.3 Software Specifications

1.4 Exploded View of the Host

Figure 1-3 shows the exploded view of the host.

Figure 1-3 Exploded view of the host



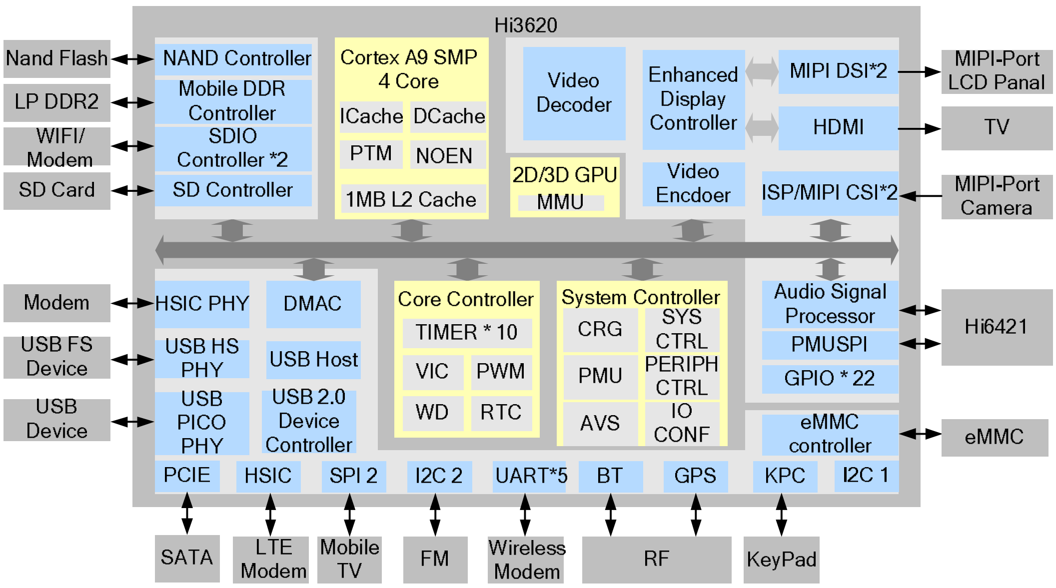
2 Functional Chips

2.1 Hi3620

The Hi3620 is a new-generation quad core ARM cortex-A9 processor launched by Hisilicon. The processor supports 1.2 GHz processing.

Figure 2-1 shows the functional blocks of the Hi3620.

Figure 2-1 Functional blocks of the Hi3620



2.1.1 Chip Specifications

Encapsulation: 11.90 mm x 11.90 mm, 576-pin BGA/CSP encapsulation, Hi3620 (IC).

2.1.2 Pin Assignment

2.1.3 Working Principles and Functions of the Hi3620

The K3V200 system uses the Hi3620 chip as its core to provide the following logical interfaces:

NAND/eMMC Interface

The Hi3620 provides 16-bit NAND interfaces. The high 8-bits are multiplexed with the eMMC interface. Therefore, it is recommended that the eight high-order bits be connected to the eMMC component and the eight low-order bits be connected to a component such as the MLC NAND or Clear NAND.

Camera Interface and LCD Interface

The Hi3620 provides three MIPI interfaces: CSI0, DSI0, and CSI_DSI1. Each interface can contain four data lanes. The Hi3620 also provides one parallel camera interface which is known as the DVP interface.

- CSI0: This interface is used for camera image capturing.
- DSI0: This interface is used for LCD display.
- CSI1_DSI1: This interface can be statically multiplexed as an LCD display interface (in the two-screen application scenario) or as an interface for camera image capturing (in 3D image pickup and master/master camera application scenarios).
- DVP: This interface is used to connect to a camera through a parallel bus. It is reserved for the front camera.

microSD Card Interface

The Hi3620 provides a dedicated microSD card slot, which complies with the SD3.0 specification and supports the SDR50 or DDR50.

NOTE

The bus clock frequency of the SDR50 is 100 MHz, and that of the DDR50 is 50 MHz.

SDIO Interface

The Hi3620 provides two SDIO buses, which comply with the SD2.0 specification and support at most the SDR25. The two buses are used to connect peripherals.

- SDIO0: This interface is the data and control interface of the AP or modem. Its signal level is 1.8 V or 2.5 V.
- SDIO1: This interface is the data and control interface of Wi-Fi. Its signal level is 1.8 V.

NOTE

The bus clock frequency of the SDR25 is 50 MHz.

UART Interface

The Hi3620 provides five UART interfaces, all of which support four-wire hardware flow control and provide the maximum baud rate of 3.25 Mbit/s. These interfaces are used to connect to peripherals.

- UART0: This UART interface is specially used for system commissioning or loading. Its signal level is 2.5 V.
- UART1: This interface is used as the data and control interface of the AP or modem. It can also be multiplexed as a GPIO interface. Its signal level is 1.8 V or 2.5 V.
- UART2: This interface is statically multiplexed with USIM and onewire signals and reserved for peripherals. Its signal level is 1.8 V.
- UART3: This interface is multiplexed with the GPS baseband bus GPS_SPI that is integrated in the Hi3620. It provides a data and control channel for external third-party GPS devices. Its signal level is 1.8 V.
- UART4: This interface is multiplexed with the Bluetooth baseband interface BT_IF that is integrated in the Hi3620. It provides a data and control channel for external third-party Bluetooth devices. Its signal level is 1.8 V.

SPI Interface

The Hi3620 supports five groups of SPI bus interfaces, all of which work in master mode.

- SPI0: This SPI interface supports a maximum of four chip selection signals. It is reserved for peripherals, such as the CMMB. Its signal level is 1.8 V.
- SPI1: This interface is the communication and control interface of the modem. Its signal level is 1.8 V or 2.5 V.
- PMU_SPI: This SPI interface is dedicated for the PMU (Hi6421) and works in three-wire mode (the input end and the output end share the same data signal). Its signal level is 1.8 V.
- BT_SPI: This interface is a dedicated SPI interface between a Bluetooth baseband unit integrated in the Hi3620 and the RF IC (Hi6350). Its signal level is 1.8 V.
- GPS_SPI: This interface is a dedicated SPI interface between a GPS baseband unit integrated in the Hi3620 and the RF IC (Hi6350). Its signal level is 1.8 V.

I2C Bus

The Hi3620 provides four groups of I2C buses. Two groups are dedicated for camera interfaces, and the other two groups are used for peripherals.

- ISP_I2C0/1: used for camera I2C interfaces.
- I2C0: used for the xSenor, capacitive touchscreen, and independent FM communication and data interfaces.
- I2C1: used for the charging IC.

NOTE

The xSensor and capacitive touchscreen are components that may be frequently accessed. Therefore, the preceding I2C bus allocation mode is applied by default but a jumper is reserved during design to connect the capacitive touchscreen to I2C1.

Digital Audio Interface PCM/I2S

The K3V200 system provides three groups of digital audio interfaces to connect to a codec inside the Hi6421.

- I2S interface: This interface is a stereo audio interface between the Hi3620 and the codec inside the Hi6421.
- M_PCM interface: This interface provides a voice channel between the modem and the codec inside the Hi6421.

- BT_PCM interface: This interface provides a voice channel between external third-party Bluetooth devices and the codec inside the Hi6421.

HDMI Interface

The Hi3620 complies with the HDMI1.3a protocol specification. It supports high-definition playing (up to 1080p) and provides HDMI interfaces to connect to external display devices.

HSIC Interface

The Hi3620 provides the HSIC interface as the active high-rate communication and control interface between the AP and the modem.

USB Interface

The Hi3620 provides two USB2.0 interfaces, both of which support the highest speed 480 Mbit/s.

- USB_NANO interface: This interface statically supports USB 2.0 hosts and devices.
- USB_PICO interface: This interface supports USB2.0 devices and BC1.1 (in compliance with a charging specification supplementary to the USB2.0 specification).

PCIe Interface

The Hi3620 supports one PCIe 1.0 interface, which is reserved for external devices, such as a South Bridge or SATA disk.

2.2 POP LPDDR2

The DDR2 chip uses the POP encapsulation technology. Currently, two vendors ELPIDA and Samsung supply this chip to Huawei.

Figure 2-2 shows the functional blocks of the POP LPDDR2 chip.

Figure 2-2 Functional blocks of the POP LPDDR2 chip

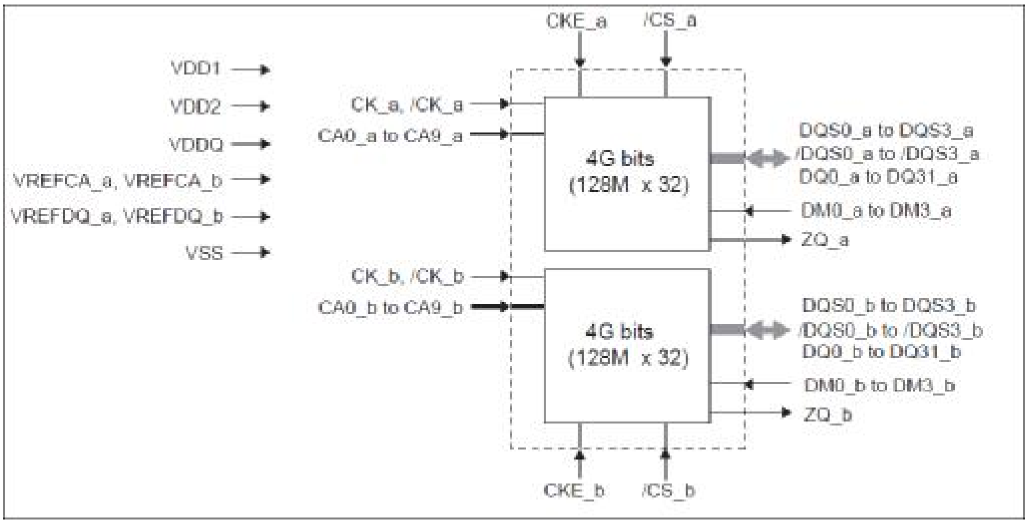
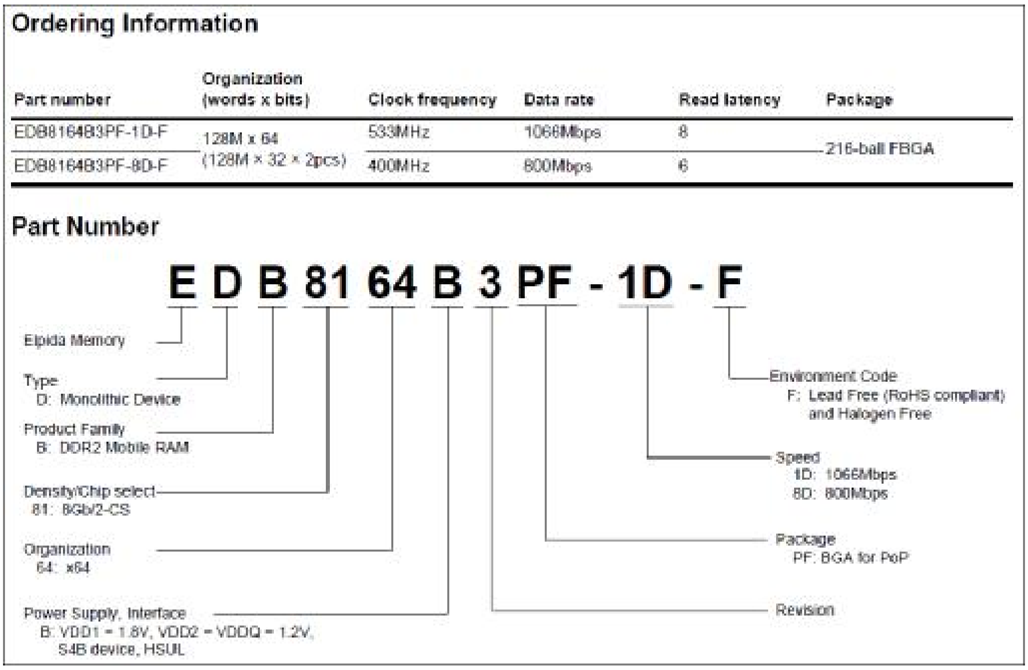


Figure 2-3 shows the model of the POP LPDDR2 chip provided by ELPIDA.

Figure 2-3 Model of the POP LPDDR2 chip provided by ELPIDA


Ordering Information

Part number	Organization (words x bits)	Clock frequency	Data rate	Read latency	Package
EDB8164B3PF-1D-F	128M x 64 (128M × 32 × 2pcs)	533MHz	1066Mbps	8	216-ball FBGA
EDB8164B3PF-8D-F		400MHz	800Mbps	6	

Figure 2-4 shows the model of the POP LPDDR2 chip provided by Samsung.

Figure 2-4 Model of the POP LPDDR2 chip provided by Samsung

Part Number	Max Freq.		Interface	Package
	A-Channel	B-Channel		
K3PE7E700M-XGC1	800Mbps (tCK=2.50ns)	800Mbps (tCK=2.50ns)	HSUL_12	12x12 216FBGA (Lead Free, Halogen Free)
K3PE7E700M-XGC2	1066Mbps (tCK=1.875ns)	1066Mbps (tCK=1.875ns)		

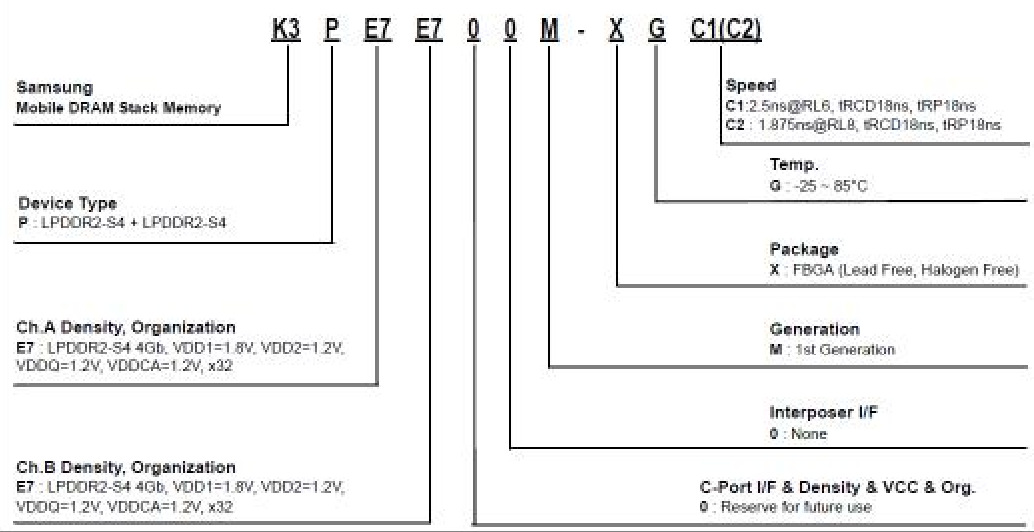
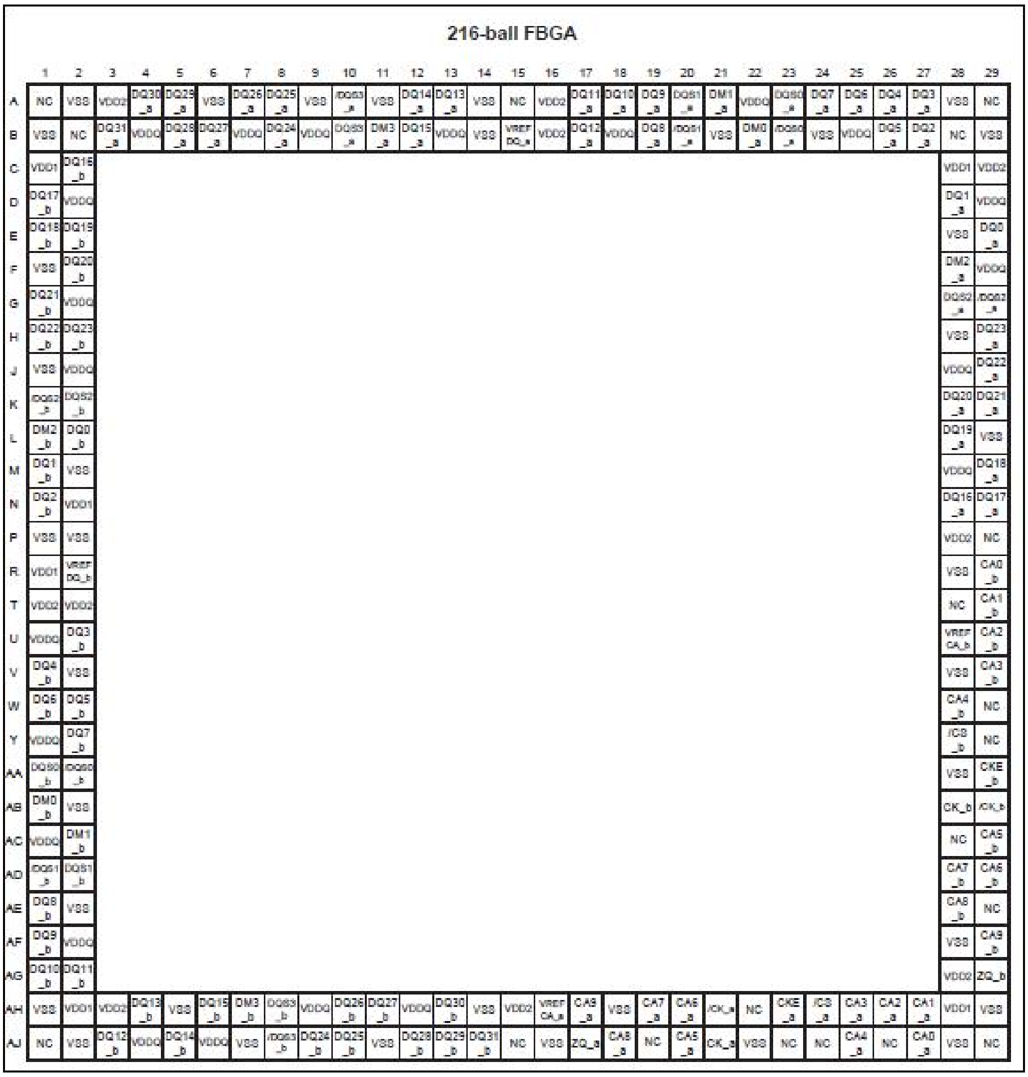


Figure 2-5 shows the pin assignment of the POP LPDDR2 chip.

Figure 2-5 Pin assignment of the POP LPDDR2 chip



2.3 PMU Hi6421

The Hi6421V200 chip is an important component of Hisilicon K3 application processor solution, which is a semiconductor solution for mobile phones. It is an integrated circuit that provides power management, audio processing, and diversified interfaces. Its functions are described as follows:

Power Supply

BUCK0 and BUCK1 serve as the primary power of the quad core A9, and output 1.1 V by default. The maximum parallel output current is 4000 mA. BUCK0 and BUCK1 are switched on or off by controlling the external hardwire signal BUCK01_EN. The output voltage is adjusted through SPI interfaces to meet the system AVS policy, so that the power consumption of the system is minimized on the precondition of guaranteed system performance.

BUCK2 serves as the primary power of the GPU, and outputs 1.1 V by default. Its maximum current is 1400 mA. SPI interfaces are applied to switch on or off BUCK2 and adjust the output voltage of BUCK2, so that the power consumption of the system is effectively controlled.

BUCK3 supplies power to the peripherals of the Hi3620, and outputs 1.1 V by default. Its maximum current is 1100 mA. BUCK3 is switched on or off by controlling the external hardwire signal BUCK3_EN.

BUCK4 supplies power to the I/O of the Hi3620 (by default the power voltage is 1.8 V) or the LP DDR2 (by default the power voltage is 1.2 V). Its maximum current is 1000 mA. The default output voltage varies according to different applications. The default output voltage is controlled by the external hardwire signal BUCK4_VC.

BUCK5 serves as the input power of LDO2 and LDO3 to improve the operating efficiency of low dropout (LDO) regulators. Its maximum current is 500 mA.

Of the 24 LDOs, 21 LDOs supply power to the following components:

- MLC NAND
- 26 MHz clock oscillation circuit
- AP system area
- DDR HPY I/O
- MIPI
- 3620 and Hi6421V200 digital I/O
- 3620 2.6 V I/O
- microSD card I/O
- USB PHY
- eFuse
- Bluetooth
- GPS
- microSD card
- CMMB
- Wi-Fi I/O
- Wi-Fi core
- LCD I/O
- LCD analog
- Camera I/O
- Camera analog
- Camera VCM

All these power channels support power saving (in dormant or ECO mode). The rest three LDOs supply power to an audio circuit (including HKADC), a PMU analog circuit, and a PMU digital circuit. The charge pump supplies power to the HDMI, and provides the backup battery charging function.

Audio Unit

The audio unit integrates a sigma-delta audio codec, which makes possible flexible resource configuration and provides abundant audio applications to meet audio processing requirements in various scenarios. The Hi6421V200 chip can connect to the AP, modem, or Bluetooth through one I2S interface and two PCM digital audio interfaces. It can also connect to peripherals through analog interfaces, such as line I/O and MIC interfaces.

Furthermore, the audio unit implements interworking and switching between audio signal resources, provides sound volume adjustment, and supports digital MIC input signals. Multiple audio amplifiers are built in the Hi6421V200 chip to drive the loudspeaker, headset, and earpiece. The headset checking function is used to identify whether the headset is installed. It helps the system save power overheads, and supports headset key detection.

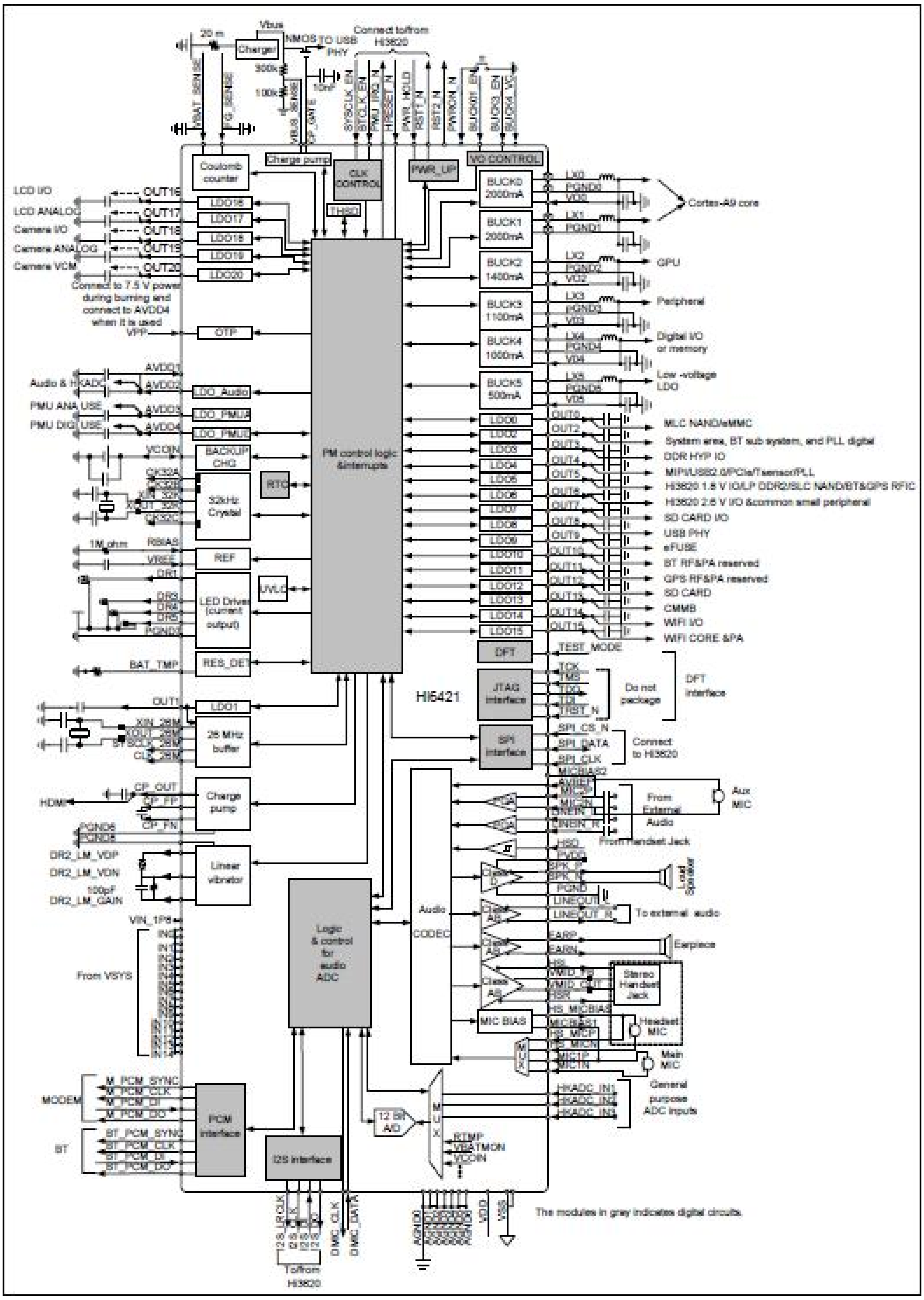
Interface Unit

The interface unit of the Hi6421V200 chip provides the following functions:

- Uses SPI interfaces to implement high-rate communication with the AP
- Provides a coulometer to detect changes to the electric energy of the battery
- Provides a 12-bit HKADC to monitor four channels of analog parameters in real time, including the voltage of the main battery, the temperature of the main battery, and the voltage of the backup coin battery.
- Provides the drive for one vibration motor or linear motor, one LED background drive (maximum current 40 mA), and three LED drives (the breathing function can be configured)
- Provides one 26 MHz clock oscillator and two output drives.
- Provides one 32.768 kHz clock oscillator and three output drives.
- Provides one interface circuit for detecting the thermistor of the main battery.

Figure 2-6 shows the functional blocks of the power supply.

Figure 2-6 Functional blocks of the power supply



The Hi6421V200 chip has the following features:

- Five high-efficiency buck-type switch power convertors

  BUCK0: 1.1 V 2000 mA for the A9 Core, supporting AVS adjustment.

  BUCK1: 1.1 V 2000 mA for the A9 Core, supporting AVS adjustment.

BUCK2: 1.1 V 1400 mA for the GPU, supporting AVS adjustment.

BUCK3: 1.1 V 1100 mA for peripherals.

BUCK4: 1.2 V or 1.8 V 1000 mA for LPDDR2 or AP I/O.

BUCK5: 1.8 V 500 mA for low-voltage LDO.

NOTE

BUCK0 and BUCK1 are connected in parallel.

- 21 external LDO linear voltage regulators and four internal LDO linear voltage regulators

  LDO0: 2.85 V @ 300 mA for MLC NAND/eMMC

  LDO1: 1.8 V @ 50 mA for 26 MHz clock oscillation circuit

  LDO2: 1.1 V @ 150 mA for the system area, Bluetooth subsystem, and digital PLL (The system in standby mode does not need to be powered off)

  LDO3: 1.2 V @ 350 mA for the DDR PHY I/O to be powered off or the HSIC PHY 1.2 V (Power-off is required)

  LDO4: 2.5 V @ 250 mA for MIPI/USB2.0/PCIe/T Sensor/PLL 2.5 V analog power (Power-off is required)

  LDO5: 1.8 V @ 300 mA for Hi3620 & Hi6421V200 1.8V I/O, LP DDR2, SLC NAND, or Bluetooth&GPS RFIC

  LDO6: 2.6 V @ 300 mA for Hi3620 2.6 V I/O and small peripherals

  LDO7: 2.6 V @ 50 mA for Hi3620 microSD card slot I/O (Dynamic switching between 1.8 V and 2.6 V is needed)

  LDO8: 3.3 V @ 200 mA for USB PHY

  LDO9: 2.6 V @ 200 mA for eFuse power supply (Power-off is required)

  LDO10: 2.85 V @ 150 mA for Bluetooth RF&PA; reserved

  LDO11: 2.85 V @ 150 mA for GPS RF&PA; reserved

  LDO12: 2.85 V @ 500 mA for the microSD card

  LDO13: 2.85 V @ 300 mA for CMMB

  LDO14: 2.85 V @ 150 mA for Wi-Fi I/O

  LDO15: 3.3 V @ 300 mA for Wi-Fi core&PA

  LDO16: 2.85 V @ 150 mA for LCD I/O

  LDO17: 2.85 V @ 150 mA for LCD Analog

  LDO18: 2.85 V @ 300 mA for Camera I/O and the input of the internal core power regulator

  LDO19: 2.85 V @ 300 mA for LCD Camera Analog

  LDO20: 2.85 V @ 300 mA for LCD Camera VCM

  LDO_Audio: 3.3 V @ 300 mA for Audio & HKADC

  LDO_PMUA: 3.15 V @ 10 mA for PMU Analog

  LDO_PMUD: 1.8 V @ 10 mA for PMU Digital

- Real-time clock (RTC) with the alarm clock function

  The Hi6421V200 chip integrates a 32.768 kHz crystal oscillator and supports three channels of clock buffer output independently controlled.

  The RTC serves as the reference time and date benchmark of the system.

  The RTC supports the alarm clock function and scheduled power-on.

  The RTC supports power supply through a backup coin battery.

- Two channels of 26 MHz high-frequency clock drive and output

  The Hi6421V200 chip integrates a 26 MHz clock oscillator drive.

  The Hi6421V200 chip is compatible with 26 MHz input clocks.
- Two channels of independent 26 MHz clock buffer output
- Four LED DC drive ports

  DR1 can be used for keypad backlight control. The drive current ranges from 5 to 40 mA.

  DR3 maps to a red LED, DR4 maps to a green LED, and DR5 maps to a blue LED. They support breath control.
- One DC or linear motor drive

  DR2 supports strong drive capability up to 250 mA.
- Three-wire SPI interfaces to communicate with the processor
- One charge pump boost converter

  The boost converter outputs a 5 V voltage and a maximum of 60 mA current.
- Built-in 12-bit HKADC to monitor physical status parameters in real time

  The 12-bit HKADC can detect the voltage of the battery.

  The 12-bit HKADC can detect the voltage of the coin battery.

  The 12-bit HKADC can detect the three channels of external analog input voltages.

  The 12-bit HKADC can detect the testability of other signals inside the chip.
- Detecting changes to the electric energy of the battery by using a coulometer
- Complete audio processing solution
- Supporting normal system power-on and operations when the main battery is not detected
- Low-power design

  The entire operating current of the chip is only 150 uA (typical value for the system in dormant state) or 30 uA (when the system is powered off and only the RTC is working).
- Over-voltage, over-heat, and over-current protection
- Operating temperature: –30°C to +85°C

2.4 Wi-Fi and Bluetooth Modules

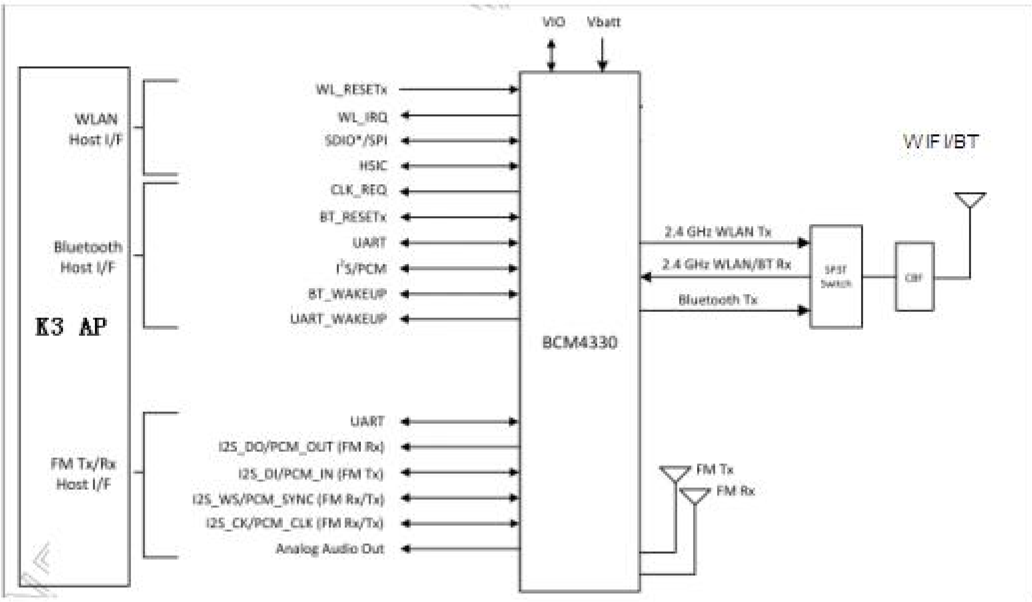
The Wi-Fi and Bluetooth modules of the S10 are designed based on the integrated chip BCM4330 according to Huawei principle of normalization for Wi-Fi design. The BCM4330 chip integrates the IEEE 802.11b/g/n 2.4 GHz or 5.1 GHz solution (RF transceiving and baseband demodulation) and a transceiver for the Bluetooth and FM modules. Signals from the Bluetooth and FM modules are output by the transceiver of the BCM4330 chip to the Hi6421 modulation and demodulation module on the AP side to implement the overall functions of the BCM4330 chip. The BCM4330 chip can use external Wi-Fi power amplifiers (PAs) or low-noise amplifier (LNAs) to improve Wi-Fi RF performance and provide higher expandability. In particular, an external PA or LNA can be deployed in subsequent version planning to improve Wi-Fi power and sensitivity to meet strict Wi-Fi RF performance requirements of TMO in North America.

In terms of RF design for Wi-Fi, Bluetooth, and FM modules, the 2.4 GHz frequency band is applied to Wi-Fi and Bluetooth modules. Both Wi-Fi and Bluetooth work in time division duplex (TDD) mode and transmit or receive signals on the same antenna under switch control.

For the FM module, a common earphone antenna is used to receive FM signals. The BCM4330 chip performs intermediate frequency (IF) conversion for FM signals, so that IF signals are demodulated on the AP side.

Figure 2-7 shows the RF solution for the Wi-Fi and Bluetooth modules of the S10.

Figure 2-7 RF solution for the Wi-Fi and Bluetooth modules of the S10



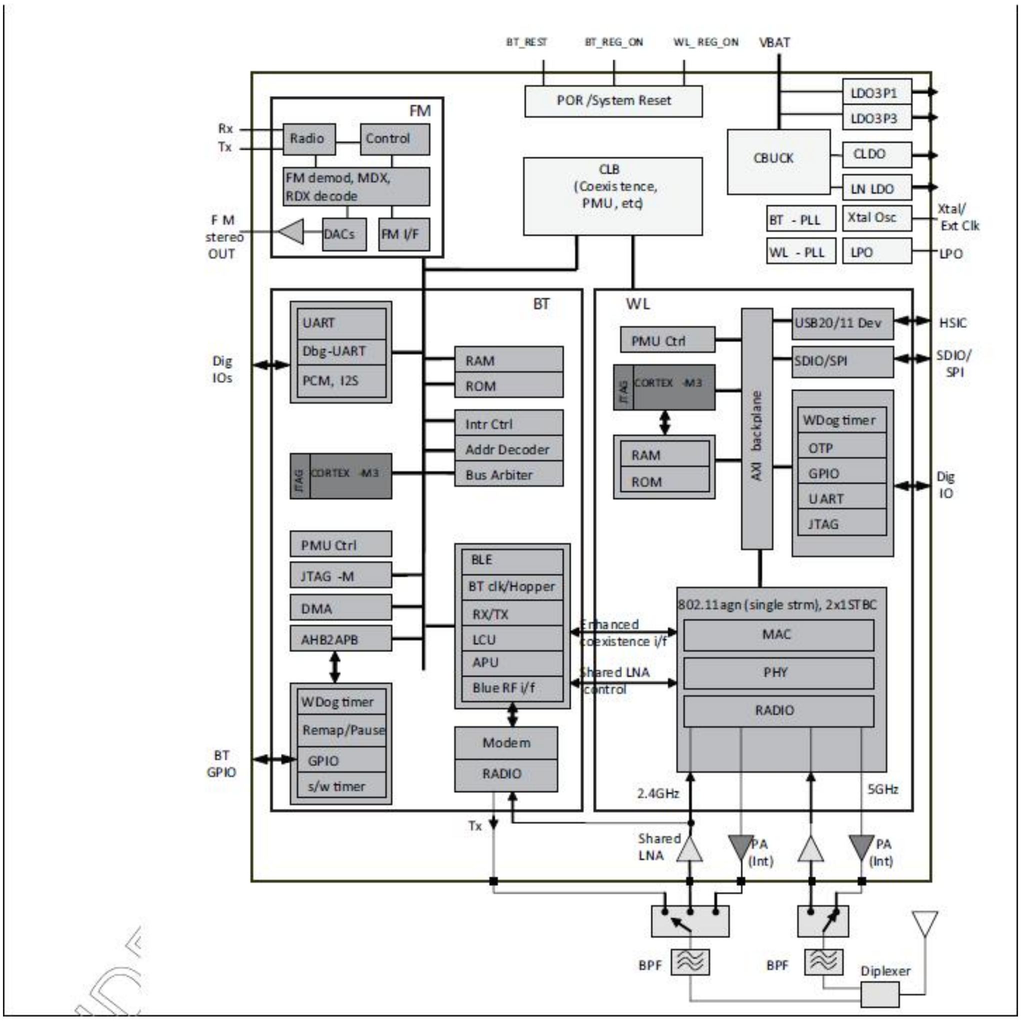
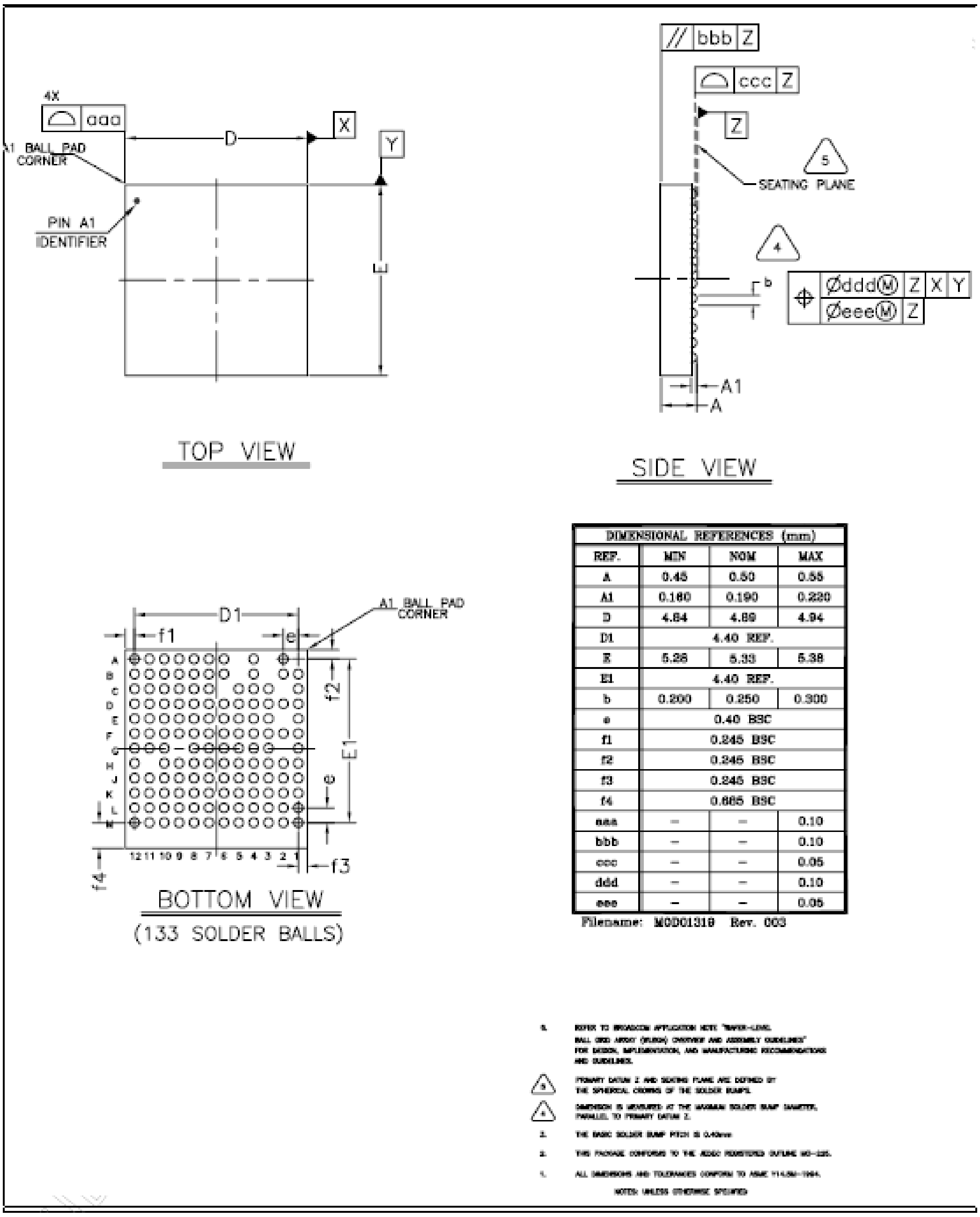


Figure 2-8 shows the components encapsulated in the WI-FI or Bluetooth module.

Figure 2-8 Components encapsulated in the WI-FI or Bluetooth module



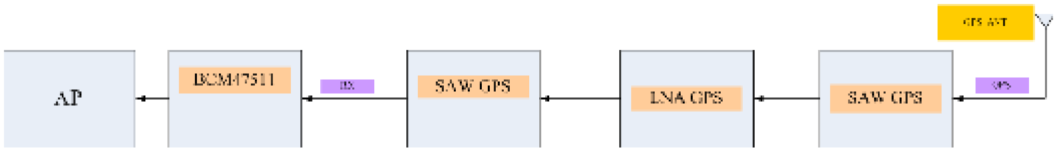
DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.160	0.190	0.220
D	4.84	4.89	4.94
D1	4.40 REF.		
E	5.28	5.33	5.38
E1	4.40 REF.		
b	0.200	0.250	0.300
e	0.40 BSC		
f1	0.245 BSC		
f2	0.245 BSC		
f3	0.245 BSC		
f4	0.665 BSC		
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

2.5 GPS BCM47511

The S10 needs to include a GPS module to implement the GNSS function. It must also be compatible with the global navigation satellite system (GLONASS). Therefore, Huawei selected the GPS chip BCM47511. The BCM47511 chip provides external GPS LNA interfaces to improve the receiving performance of the GPS module.

Figure 2-9 shows the functional blocks of the RF solution for the GPS module of the S10. After the GPS antenna receives signals from the GPS or GLONASS, SAW filtering is performed before signals are amplified by an LNA. Then SAW filtering is performed again before signals are input to the BCM47511 for further processing.

Figure 2-9 RF solution for the GPS module of the S10



The BCM47511 chip has the following features:

- The BCM47511 SoC solution uses an independent new-generation GPS receiver developed by Broadcom. This GPS receiver integrates the functions of both the GPS and the GLONASS. The BCM47511 chip is compatible with pins in the popular BCM4751 SoC solution launched by Broadcom. Therefore, customers can quickly upgrade products to support the GLONASS.
- The GPS kernel of the BCM47511 chip, based on a host system architecture, splits the processing function into two parts which are separately implemented by the GPS chip and the main system CPU. This obviously reduces system costs. In addition, the GPS or GLONASS software algorithm used on the main system can be customized or optimized when necessary. After splitting the processing function into two parts, the GPS receiver of the BCM47511 chip can perform most dense computation tasks, so that the software on the main system needs only to perform the ultimate calculation.
- The BCM47511 chip consumes little power and provides an ultra-low-power tracing mode. It integrates LDO voltage regulators to provide a temperature-compensated crystal oscillator (TCXO) for the GNSS. The BCM47511 chip can also have LNAs to lower the total material cost. Broadcom provides GPS location library APIs and GPS protocol client software, so that designers can make full use of the advanced functions of the BCM47511 chip.
- The Bluetooth kernel of the BCM47511 chip is optimized to attain low power consumption. This kernel also maintains high receiver sensitivity and complies with the Bluetooth 4.0 specification.

Figure 2-10 shows the functional blocks of the BCM47511 chip.

Figure 2-10 Functional blocks of the BCM47511 chip

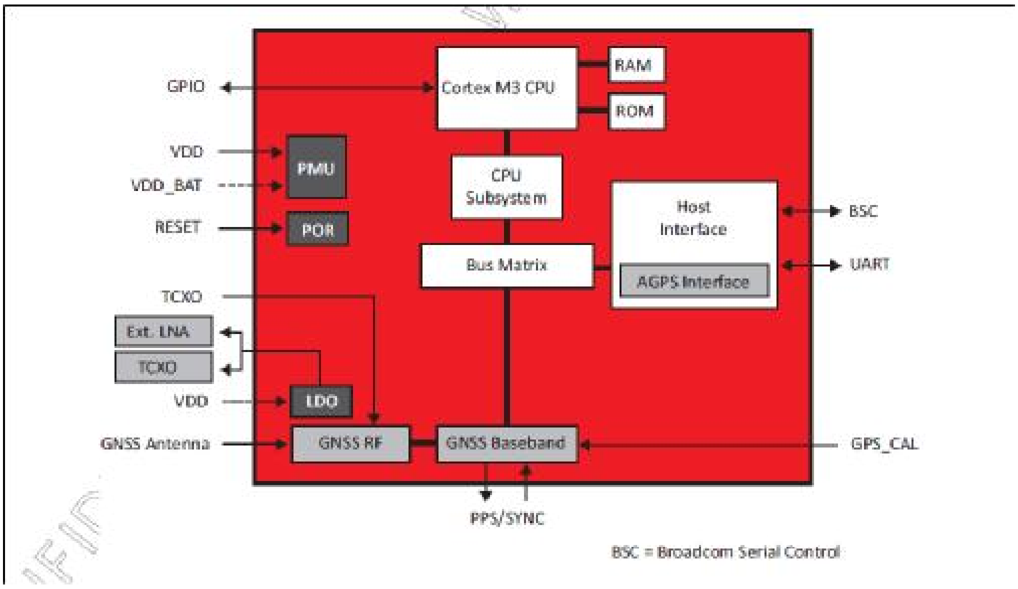


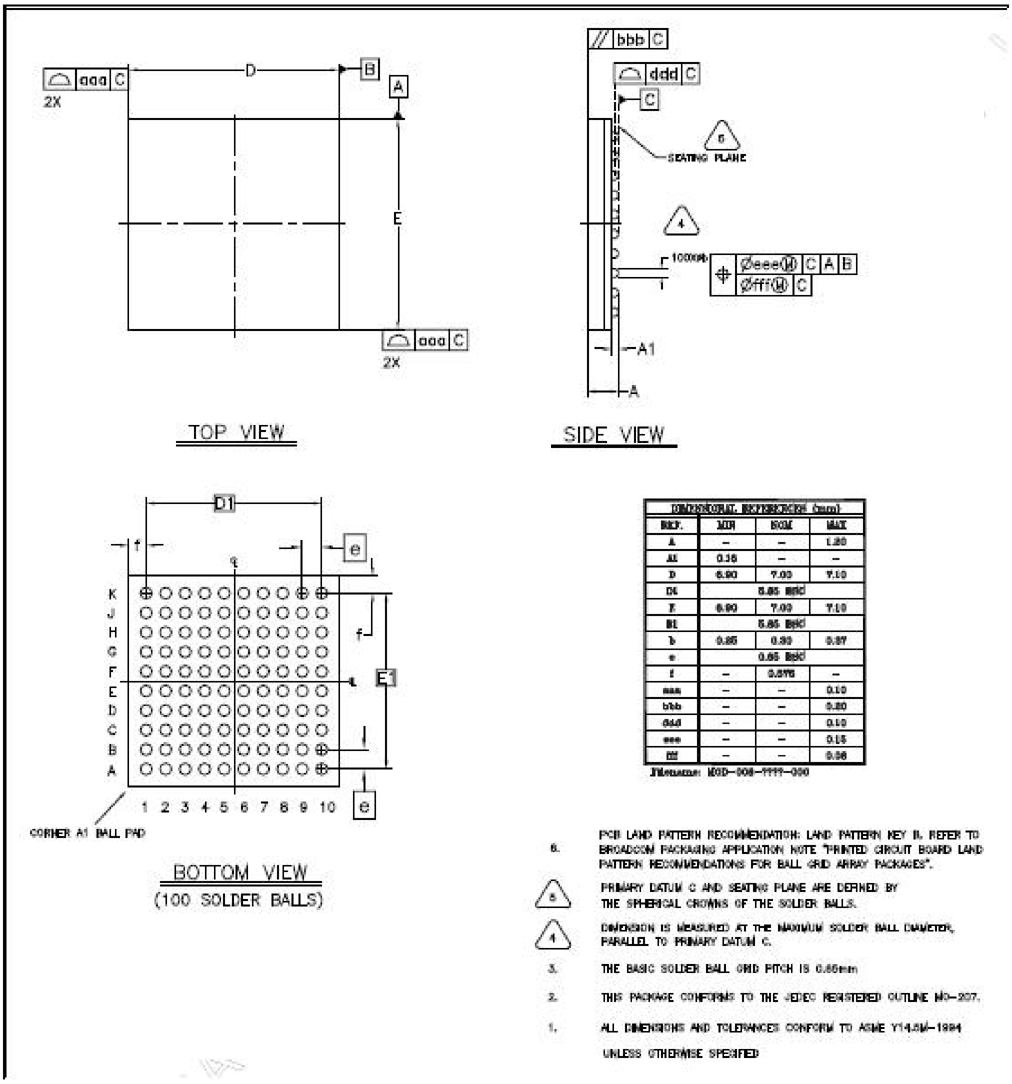
Figure 2-11 shows the available models of the BCM47511.

Figure 2-11 Models of the BCM47511

Part Number	*Package*	*Packing*	*Minimum Order Quantity*
BCM47511IFBG	100-pin FBGA	Tape-and-reel	2,500
BCM47511IUBG	42-pin WLBGA	Tape-and-reel	5,000
BCM47511IUB2G[a]	42-pin WLBGA	Tape-and-reel	5,000

Figure 2-12 shows the components encapsulated in the BCM47511 chip.

Figure 2-12 Components encapsulated in the BCM47511 chip



REF.	MIN	NOM	MAX
A	–	–	1.20
A1	0.16	–	–
D	6.90	7.00	7.10
D1		5.85 BSC	
E	6.90	7.00	7.10
E1		5.85 BSC	
b	0.25	0.30	0.37
e		0.65 BSC	
f	–	0.575	–
aaa	–	–	0.10
bbb	–	–	0.20
ddd	–	–	0.10
eee	–	–	0.15
fff	–	–	0.08

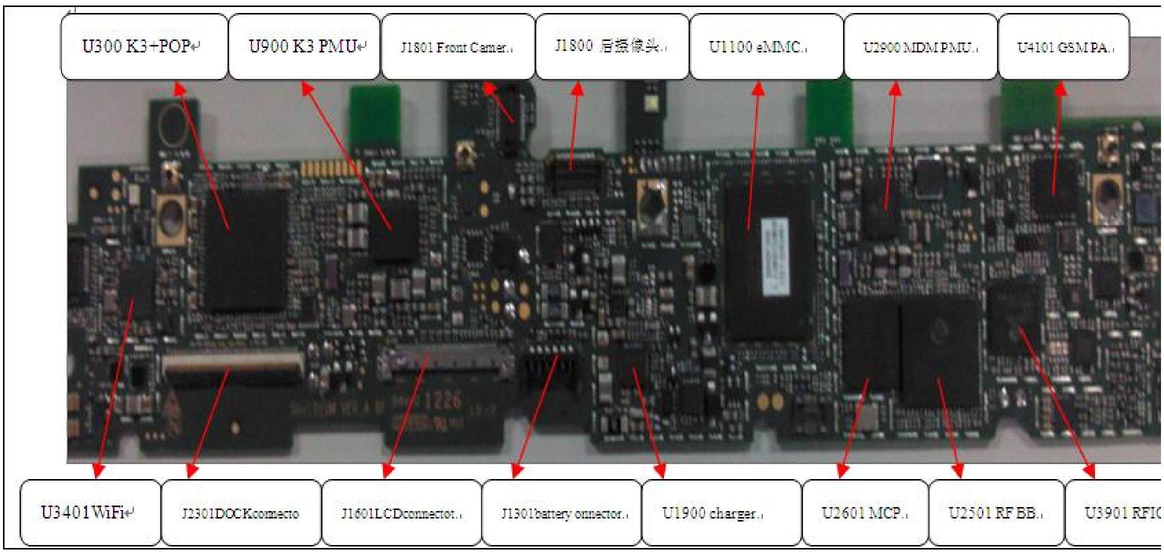
Filename: MOD-008-????-000

3 Layout of Major Components

3.1 Layout of Components on the S10 PCBA

Figure 3-1 shows the layout of components on the S10 PCBA.

Figure 3-1 Layout of components on the S10 PCBA



3.2 Components on the S10 PCBA

Table 3-1 lists the components on the S10 PCBA.

Table 3-1 Description of components on the S10 PCBA

BOM Number	Description	Remarks
14240181	BTB Connector,Fmale,24Pin,0.4mm,SMT,Mating Height 1.0 mm,Terminal Dedicated	J2105

BOM Number	Description	Remarks
14090087	Soft Print Board Connector,40Pin,0.5mm,0.5mm,0.3mm,Terminal Dedicated	J2301
39210010	Terminal Baseband process IC,Single Band 2.4GHz WLAN/ Bluetooth 2.1/FM Single chip-BCM4330,2.3~5.5V,WLBGA133(Pb-free)	U3401
35020160	Consumption Chip,Hi3620GFCV111G12,FCCSP 576,1.1/1.2/ 1.8/2.6/3.3V,Application processor	U300
40020172	DDR2 DRAM,8Gb LPDDR2,533MHz,32bit,1.8V/1.2V,216BALL FBGA(POP),Terminal Dedicated	U300_POP
35020158	Consumer Chips-Hi6421GFCV231-FCCSP189-1.8/3.3/4.2V-K3 PMU and Codec chip	U900
14240470	Card Block Connector,female,40,0.4mm,Micro Coaxial Connector,Terminal Dedicated	J1601
38140024	Semiconductor Sensor,E-Compass,WL-CSP(Pb-free),3axis,Terminal Dedicated	U2005
38140020	Semiconductor Sensor,three-axis gyroscope,SMT	U2003
38140023	Semiconductor Sensor,Accelerometer,LGA,3axis,Terminal Dedicated	U2003
51621274	DKBA8.382.0615,Main Antenna SMT Spring,C5600	J100, J1000, J1001, J1002, J1003, J3503, J3504, J3601, J3602, J3802, J3804, J3805
14240533	IO Connector,WTB Connector,6pin,single row,Terminal Dedicated	J1301
39070073	-0.3~2.75V,Battery Gauge,SON,Terminal Dedicated	U1301
39070085	Battery Management IC,4.1~16V,DC-DC Charger,Smart Power Control,QFN,SMT,Terminal Dedicated	U1900
40060318	NAND Flash, 16GB EMMC V4.4, 52MHz, 1024KB, 3.3V, FBGA169(Pb-Free),Terminal Dedicated	U1100
40060344	MCP, 2Gb(256M*8bit) NAND,23MHz,128KB,1.8V,VFBGA130(Pb-free),1G (32M*32bit) Mobile LPDDR SDRAM,Balong Dedicated,Terminal Dedicated	U2601
51623731	DKBA80359313,S7-931U-POWER-FRAME	J2502
51623727	DKBA80359309,RGB-FRAME,S7-931U	J2503

BOM Number	Description	Remarks
51623736	DKBA80359318,S7-931U-WIFI-FRAME	J2504
51623733	DKBA80359315,S7-931U-CODEC-FRAME	J2505
51623729	DKBA80359311,S7-931U-FLASH-FRAME	J2506
51623725	DKBA80359307,BB-FRAME,S7-931U	J2507
12070038	Temperature Compensated Oscillator,26MHz,+/-1.5ppm(max),+1.8V,+/-0.5ppm(max),-40degC,85degC,Terminal Dedicated	TCXO2300
39200455	Terminal Baseband process IC,Digital Base Band Processor-1.2GHz-RK2918,1.2/1.8/2.6/2.5/3.3V,TFBGA512,Terminal De dicated	U4
39110682	LDO,2.5V,2%(Max),0.3A,SOT23-5,Terminal dedicated	U1000
39110548	LDO,3.3V,2%,0.15A,SC70-5,Terminal Dedicated	U1001, U1300
39110490	Voltage Regulator,1.2V LDO Regulator,2%,0.15A,SOT-23-5 A,Terminal Dedicated,BT	U1002
39110471	Voltage Regulator,2.85,3%,0.15A,SOT-23-5,Terminal Dedicat ed (from39110307)	U1200
43140104	Interface Controller,RGB to LVDS,1.8/3.3V, Terminal Dedic ated	U1301
40060386	NAND Flash, 8GB(x8bit) MLC,40MHz,8192KB,3.3V,TSOP4 8(Pb-Free),S7-Lite Dedicate,Terminal Dedicated	U1302
36020411	CMOS,8BIT Level Shifter With Automatic Direction Sensin g,SDIO Bus Application,WCSP20,7ns,50mA,CMOS,CMOS,2 5nS,Terminal Dedicated,117C/W	U1500
36020401	CMOS,2BIT-1.8V/3.3V Level Shifter,GFN8(Pb-free),1.5ns,14 mA,CMOS,Open drain,Terminal Dedicated	U1501, U6002
43110077	AUDIO Chip,QFN,CODEC,Support I2S,PCM Interface,ACE, Terminal Dedicated	U1600
39080127	Operation Amplifier,Audio Power Amplifier,2.5V~5.5V,Diffe rencial,Micro SMD 9pin(BGA Pb-Free),Terminal Dedicated	U1700
39110709	Power Driver,2A Boost DCDC,QFN10,Terminal Dedicated	U1702
32050033	Vibrator,Cylindrical,3.0V,0.11A,11000rpm,10.5mm*4.5mm*4.85mm,SMT, SANYO, 28.5ohm,Terminal Dedicated	U1703
39070073	-0.3~2.75V,Battery Gauge,SON,Terminal Dedicated	U1800

BOM Number	Description	Remarks
39070117	Battery Management IC, 4.2V,18V,Charger with separate Po wer Path Control,WCSP,SMT,Terminal Dedicated	U1801
38140064	Semiconductor Sensor,Accelerometer,LGA,3axis,Terminal Dedicated	U1900
39070145	Voltage Monitor,2.7V, Delay Reset Chip,0.9V-6V,SOT23-3,T erminal Dedicated	U2000
47140049	RF Switch,0.5~3.0 GHz,SP3T,0.45dB,1.22,20dB,TSON,200~2 60V(HBM),Terminal Dedicated	U2100
39210036	Terminal Baseband Peripheral IC,GPS Receiver,support GLO NESS,2.3~5.5V-WLBGA42(Pb-free),Terminal Dedicated	U2300
47090053	RF LNA,1575MHz,14dB min.,1.6dB max.,SOT886,Terminal Dedicated	U2301
36020366	CMOS,4BIT Level Shifter With Automatic Direction Sensin g,WLCSP(Pb-free),7.4ns,50mA,CMOS,CMOS,Terminal Dedic ated	U2400
51078365	MU509-b,HSDPA/WCDMA 2100/900 EDGE/GPRS/GSM Fo ur Band,China Hubei Open Market,Module,Media Pad	U2401
40020189	DDR3 DRAM,2Gb DDR3,1600MHz,8bit,1.5V,FBGA78,Term inal Dedicated	U5000, U5001, U5002, U5003
39130135	RTC,Real Time Clock,TSSOP8, Terminal Dedicated	U6000
38020033	Analog Switch,Single Channel Bidirectional,1.65-5.5V,7~50o hm,250MHz,SC-70,SC-88	U6001
36020336	LVCMOS-Unbuffer Single Inverter Gate-SC-70-9ns-4mA-CMOS-CMOS	U6003
39110566	Switching Regulators,1~4V,1.5A,SMT,Terminal Dedicated	U9000, U9001, U9002, U9003
36020382	CMOS-Power on reset-MLP-8 2 x 2 x 0.8mm,0.5mm Pitch-300ns-0.5mA-COMS-COMS-3ns	U9004
12020216	Crystal,37.4MHz,10pF/8.3pF/9pF,+/-10ppm,80ohm,2016,Term inal Dedicated	X2100
12020125	Crystal,0.032768MHz,12.5pF+/-30ppm,60/80kohm,3.2*1.5 S MD,Terminal Dedicate,ELOM,TS16949	X6000

BOM Number	Description	Remarks
12020171	Crystal Oscillator,27MHz,12pF,20 ppm,50ohm,3225	X6001
12020151	Crystal,24.000MHz,12pf,+/-v30ppm,50ohm,HCX-3SB,Terminal Dedicated	X6002

4 Principles and Failure Analysis

4.1 Working Principles of the MediaPad 10 FHD

The MediaPad 10 FHD consists of a PCBA, a small I/O board, and a small headset board.

The PCBA is designed based on a combination of the AP (Hisilicon K3V200) and the Balong V7 modem. The BCM4330 solution developed by Broadcom is used for the Wi-Fi and Bluetooth modules. The GPS implements the functions of both the AGPS and the GLONESS. Currently, the GPS can already provide basic functions but temporarily there is no specific test specification for it. The BCM47511 solution launched by Broadcom is applied to the GPS. The MediaPad 10 FHD uses the K3V200 system, to which the modem Balong V7, BCM4330, BCM47511, and other subsystems are attached. There is an independent storage module for both the AP and the modem. The 16 Gbit LP DDR RAM provides a memory unit for the AP program. System and application programs are stored in a large-capacity eMMC. The modem module has an independent storage unit and memory to store related data and guarantee its normal operations. An independent PMU is designed for both the AP and the modem to separately supply power to them. That is, the power management IC Hi6421 supplies power to the AP, and the power management IC Hi6451 supplies power to the modem. When a power-on event is triggered, the power management IC Hi6421 is powered on first. After the AP system is started, the power-on process starts on the Hi6451 so that the modem system is started.

Figure 4-1 shows the functional blocks of the PCBA.

Figure 4-1 Functional blocks of the PCBA

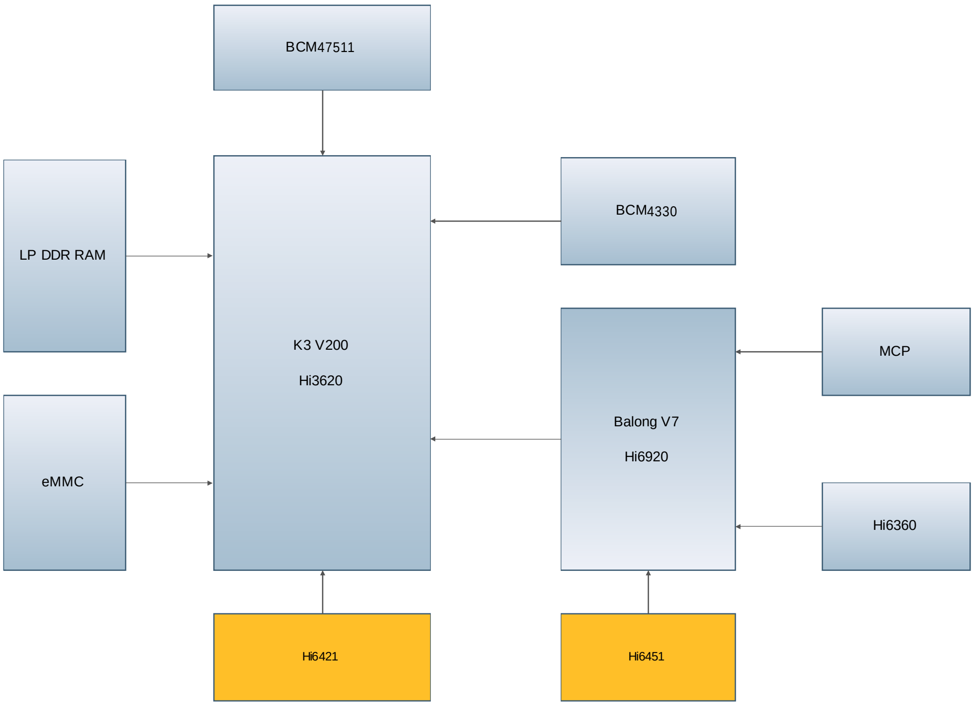


Figure 4-2 shows the layout of components on the PCBA.

Figure 4-2 Layout of components on the PCBA

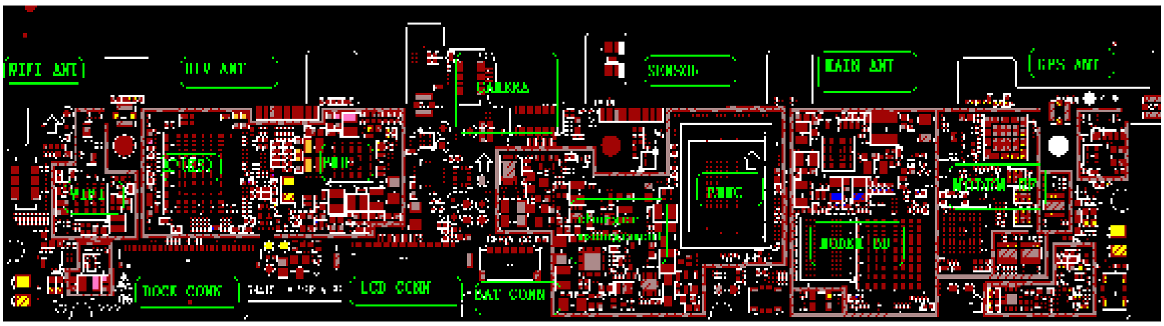
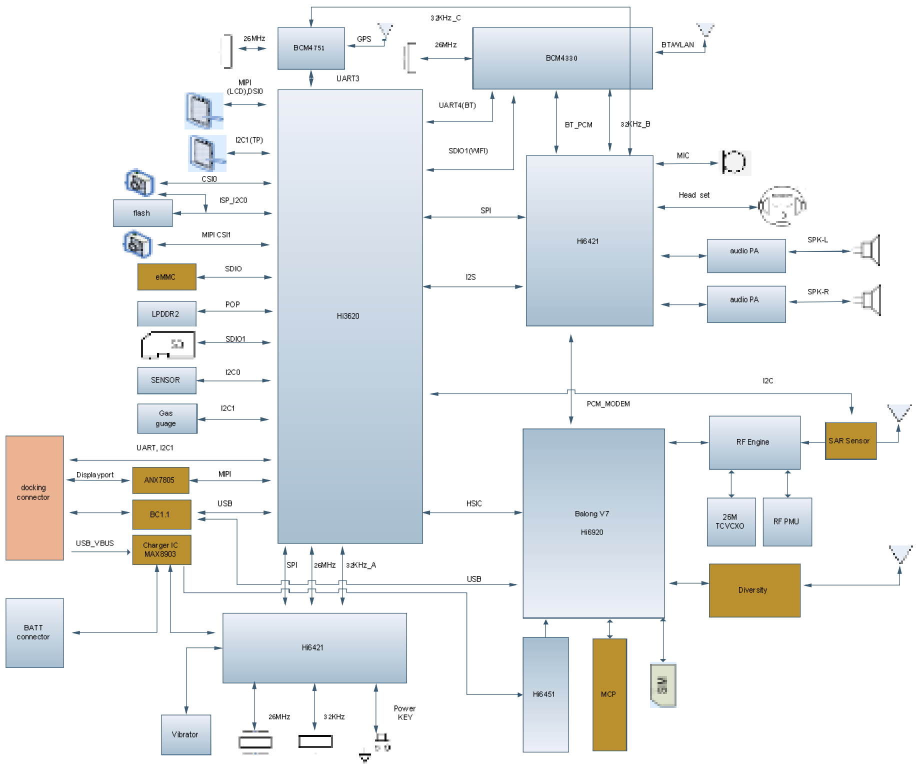


Figure 4-3 shows the physical architecture of the PCBA, where the interface connections of various modules are indicated. The application processor Hi3620 has three MPI interfaces. The CSI interface is connected to the LCD module. The CSI0 interface is connected to the rear camera. The rest MIPI interface is a multiplexing of DSI and CSI to provide digital connections for the front camera.

A 32-bit parallel bus is designed to transmit data between the LP DDR RAM and the CPU system, and the eMMC uses an 8-bit SDIO parallel port for data transmission. The PMU and codec are integrated in the Hi6421. The Hi3620 controls power settings through the SPI interface. The Wi-Fi data link is established on a 4-bit SDIO interface. The GPS and Bluetooth modules involve a small data volume, using the high-rate serial port UART as the data transmission channel.

Brand-new HSIC interfaces are used to provide high-rate data channels before the AP and the modem. The interface rate is up to 480 MHz. High-rate serial ports (HSUART) serve as auxiliary control channels. The memory unit consists of a 32-bit parallel bus, and the storage unit uses 16-bit parallel ports. External sensors, such as the acceleration sensor, compass, and gyroscope sensor, are connected to the system through I2C interfaces.

Figure 4-3 Physical architecture of the PCBA



4.2 Power-On and Power Tree

4.2.1 Hardware Startup Process

Figure 4-4 shows a power-on and power-off sequencing diagram.

Figure 4-4 Power-on and power-off sequencing

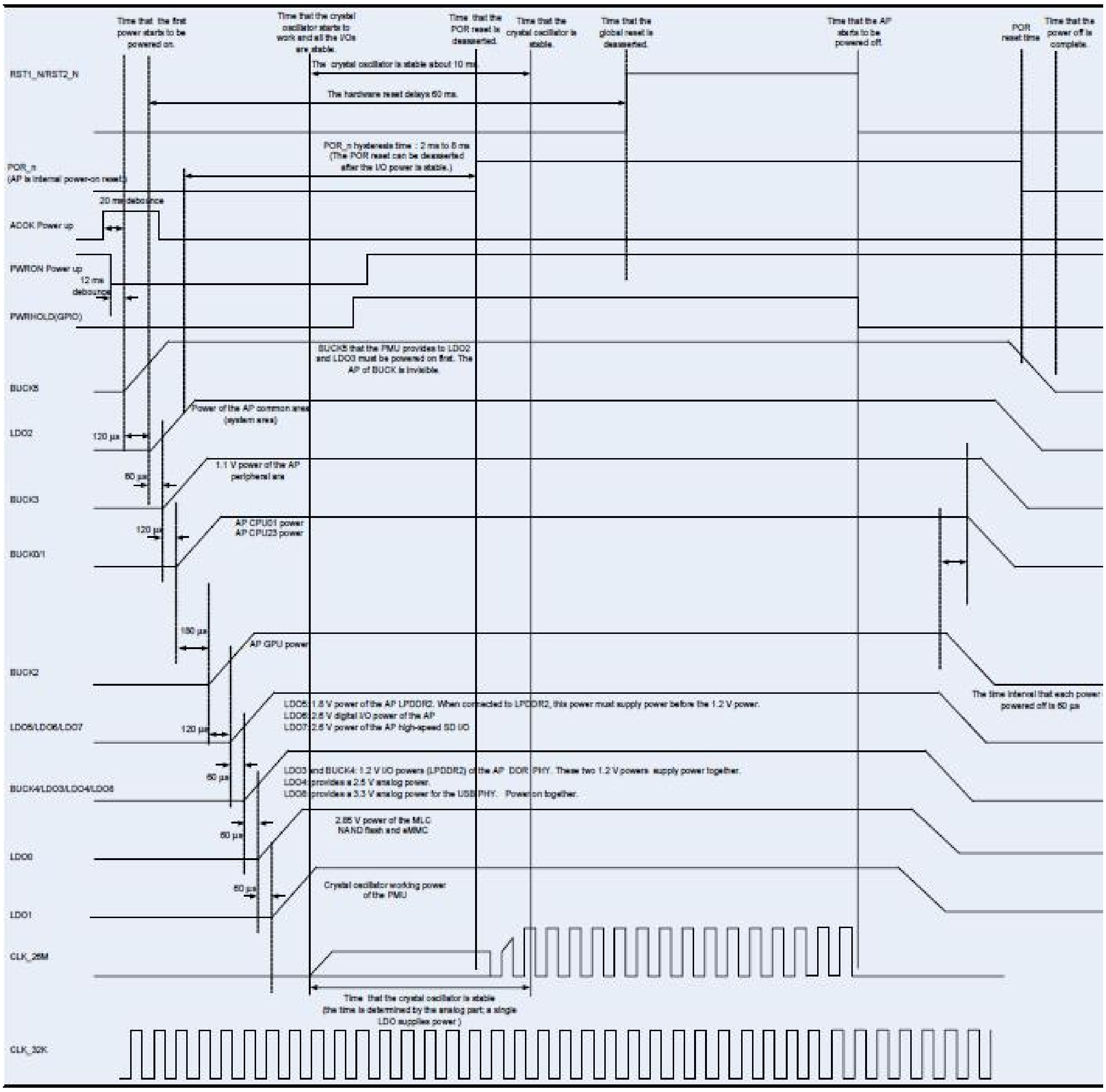
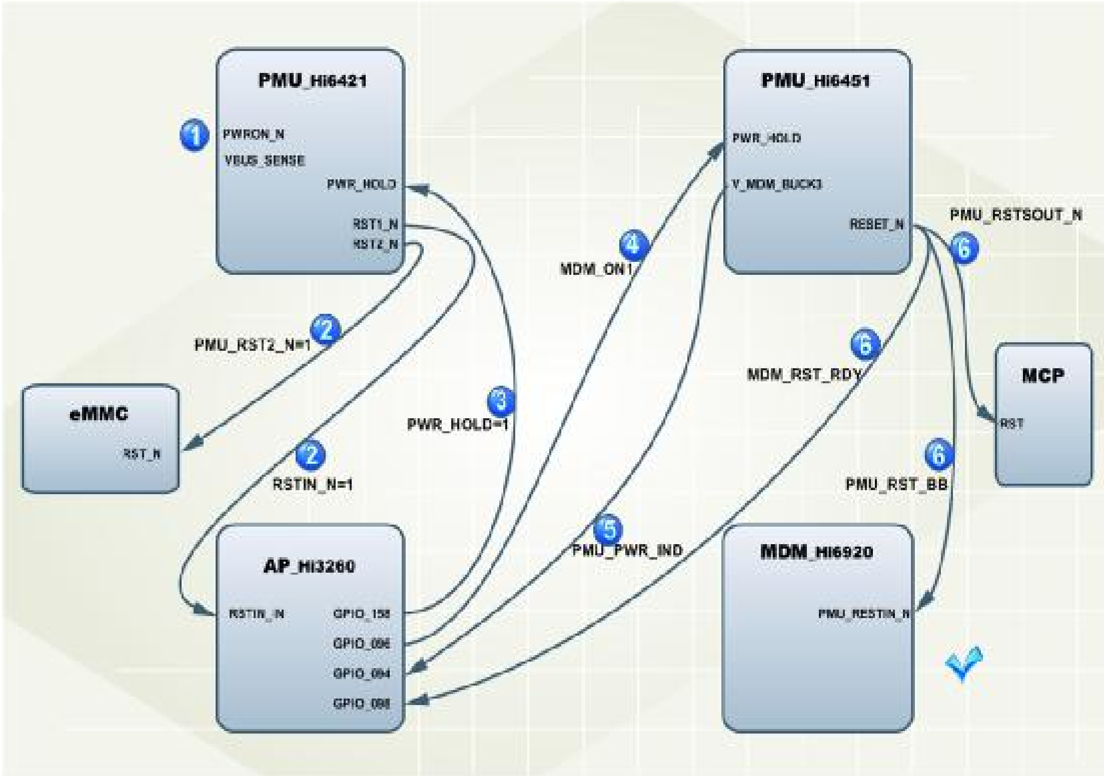


Figure 4-5 shows the power-on procedure.

Figure 4-5 Power-on procedure



The power-on process consists of the following steps:

1. A power-on event is triggered.
2. The AP_PMU sends two reset signals, one to the AP and the other to the eMMC.
3. The AP returns a HOLD signal to the AP_PMU after being reset.
4. The AP sends a power-on signal to the MDM_PMU to trigger the power-on of the MDM_PMU.
5. The MDM_PMU BUCK3 returns a PWR_OK signal to the AP after being powered on.
6. The MDM_PMU sends a reset signal to reset the MCP and MDM, and sends a notification to the AP, indicating that the MDM is ready following the reset.

4.2.2 Power Tree

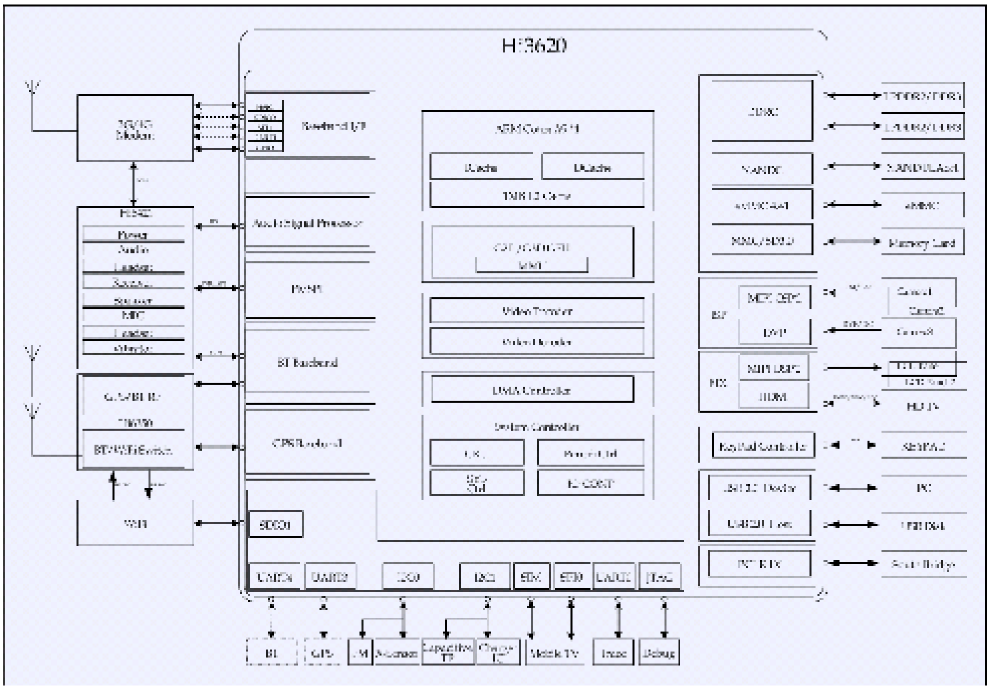
MediaPad 10 FHD Maintenance Manua

4.3 Circuit Analysis and Troubleshooting for Functional Units

4.3.1 Working Principles of the AP Subsystem

Figure 4-6 shows the AP framework.

Figure 4-6 AP framework



The K3V200 system uses the Hi3620 chip as its core to provide the following logical interfaces:

NAND/eMMC Interface

The Hi3620 provides 16-bit NAND interfaces. Of the 16-bit width, the eight high-order bits are multiplexed with the eMMC interface. Therefore, it is recommended that the eight high-order bits be connected to the eMMC component and the eight low-order bits be connected to a component such as the MLC NAND or Clear NAND.

Camera Interface and LCD Interface

The Hi3620 provides three MIPI interfaces: CSI0, DSI0, and CSI_DSI1. Each interface can contain four data lanes. The Hi3620 also provides one parallel camera interface which is known as the DVP interface.

- CSI0: This interface is used for camera image capturing.
- DSI0: This interface is used for LCD display.

- CSI1_DSI1: This interface can be statically multiplexed as an LCD display interface (in the two-screen application scenario) or as an interface for camera image capturing (in 3D image pickup and master/master camera application scenarios).
- DVP: This interface is used to connect to a camera through a parallel bus. It is reserved for the front camera.

microSD Card Interface

The Hi3620 provides a dedicated microSD card slot, which complies with the SD3.0 specification and supports at most the SDR50 or DDR50.

NOTE

The bus clock frequency of the SDR50 is 100 MHz, and that of the DDR50 is 50 MHz.

SDIO Interface

The Hi3620 provides two SDIO buses, which comply with the SD2.0 specification and support at most the SDR25. The two buses are used to connect peripherals.

- SDIO0: This interface is the data and control interface of the AP or modem. Its signal level is 1.8 V or 2.5 V.
- SDIO1: This interface is the data and control interface of Wi-Fi. Its signal level is 1.8 V.

NOTE

The bus clock frequency of the SDR25 is 50 MHz.

UART Interface

The Hi3620 provides five UART interfaces, all of which support four-wire hardware flow control and provide the maximum baud rate of 3.25 Mbit/s. These interfaces are used to connect to peripherals.

- UART0: This UART interface is specially used for system commissioning or loading. Its signal level is 2.5 V.
- UART1: unused.
- UART2: This interface is statically multiplexed with USIM and onewire signals and reserved for peripherals. Its signal level is 1.8 V.
- UART3: This interface is multiplexed with the GPS baseband bus GPS_SPI that is integrated in the Hi3620. It provides a data and control channel for external third-party GPS devices. Its signal level is 1.8 V.
- UART4: This interface is multiplexed with the Bluetooth baseband interface BT_IF that is integrated in the Hi3620. It provides a data and control channel for external third-party Bluetooth devices. Its signal level is 1.8 V.

SPI Interface

The Hi3620 supports five groups of SPI bus interfaces, all of which work in master mode.

- SPI0: This SPI interface supports a maximum of four chip selection signals. It is reserved for peripherals, such as the CMMB. Its signal level is 1.8 V.
- SPI1: This interface is the communication and control interface of the modem. Its signal level is 1.8 V or 2.5 V.

- PMU_SPI: This SPI interface is dedicated for the PMU (Hi6421) and works in three-wire mode (the input end and the output end share the same data signal). Its signal level is 1.8 V.
- BT_SPI: This interface is a dedicated SPI interface between a Bluetooth baseband unit integrated in the Hi3620 and the RF IC (Hi6350). Its signal level is 1.8 V.
- GPS_SPI: This interface is a dedicated SPI interface between a GPS baseband unit integrated in the Hi3620 and the RF IC (Hi6350). Its signal level is 1.8 V.

I2C Bus

The Hi3620 provides four groups of I2C buses. Two groups are dedicated for camera interfaces, and the other two groups are used for peripherals.

- ISP_I2C0/1: used for camera I2C interfaces.
- I2C0: used for the xSenor, capacitive touchscreen, and independent FM communication and data interfaces.
- I2C1: used for the charging IC.

NOTE

The xSensor and capacitive touchscreen are components that may be frequently accessed. Therefore, the preceding I2C bus allocation mode is applied by default but a jumper is reserved during design to connect the capacitive touchscreen to I2C1.

Digital Audio Interface PCM/I2S

The K3V200 system provides three groups of digital audio interfaces to connect to a codec inside the Hi6421.

- I2S interface: This interface is a stereo audio interface between the Hi3620 and the codec inside the Hi6421.
- M_PCM interface: This interface provides a voice channel between the modem and the codec inside the Hi6421.
- BT_PCM interface: This interface provides a voice channel between external third-party Bluetooth devices and the codec inside the Hi6421.

HDMI Interface

The Hi3620 complies with the HDMI1.3a protocol specification. It supports high-definition playing (up to 1080p) and provides HDMI interfaces to connect to external display devices.

HSIC Interface

The Hi3620 provides the HSIC interface as the active high-rate communication and control interface between the AP and the modem.

USB Interface

The Hi3620 provides two USB2.0 interfaces, both of which support the highest speed 480 Mbit/s.

- USB_NANO interface: This interface statically supports USB 2.0 hosts and devices.
- USB_PICO interface: This interface supports USB2.0 devices and BC1.1 (in compliance with a charging specification supplementary to the USB2.0 specification).

4.3.2 Detailed Analysis of Working Principles of the AP Subsystem

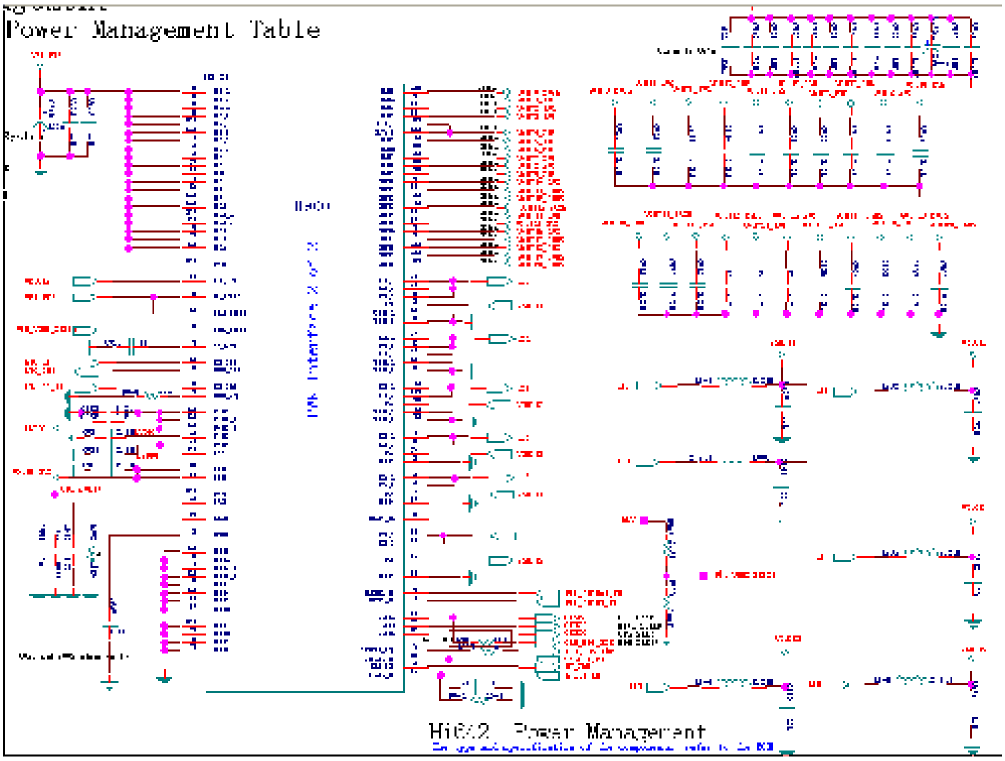
Working Principles of the AP Power Circuit

- Working principles

  The power management of the K3 Hi3620 is implemented by a dedicated power management IC Hi6421. The power supply of the AP and that of some peripherals are obtained from the Hi6421.

Figure 4-7 shows the working principles of the PMU.

Figure 4-7 Working principles of the PMU



- Circuit analysis

  The HI6421 converts the primary power voltage VHP_PWR into various voltages during power-on.

Table 4-1 lists these voltages.

Table 4-1 Voltage signals of the AP power circuit

Signal Name	Default Voltage	Programmable Voltage Range	Maximum Current	Default Status
BUCK0/1	1.1 V	0.7–1.60, 128 steps, best efficiency point = 400 mA	2.0 A	ON
BUCK2	1.1 V	0.7–1.60, 128 steps, best efficiency point = 400 mA	1.4 A	ON

Signal Name	Default Voltage	Programmable Voltage Range	Maximum Current	Default Status
BUCK3	1.1 V	0.7/0.8/0.9/0.95/1.05/1.10/1.15/1.20, best efficiency point = 300 mA	1.1 A	ON
BUCK4	1.2 V or 1.8 V	1.15/1.2/1.25/1.35/1.7/1.8/1.9/2.0, best efficiency point = 300 mA	1.0 A	ON
BUCK5	1.8 V	1.15/1.2/1.25/1.35/1.6/1.7/1.8/1.9, best efficiency point = 150 mA	500 mA	ON
LDO0	2.85 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	300 mA	ON
LDO1	1.8 V	1.7/1.8/1.9/2.0	50 mA	ON
LDO2	1.10 V	1.05/1.10/1.15/1.20/1.25/1.3/1.35/1.4	150 mA	ON
LDO3	1.20 V	1.05/1.10/1.15/1.20/1.25/1.3/1.35/1.4	350 mA	ON
LDO4	2.50 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	250 mA	ON
LDO5	1.80 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	300 mA	ON
LDO6	2.60 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	300 mA	ON
LDO7	2.60 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	50 mA	ON
LDO8	3.30 V	1.5/1.8/2.4/2.6/2.7/2.85/3.0/3.3	200 mA	ON
LDO9	2.60 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	200 mA	OFF
LDO10	2.85 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	150 mA	OFF
LDO11	2.85 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	150 mA	OFF
LDO12	2.85 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	500 mA	OFF
LDO13	2.85 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	300 mA	OFF
LDO14	2.85 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	150 mA	OFF
LDO15	3.30 V	1.5/1.8/2.4/2.6/2.7/2.85/3.0/3.3	300 mA	OFF
LDO16	2.85 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	150 mA	OFF
LDO17	2.85 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	150 mA	OFF
LDO18	2.85 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	300 mA	OFF
LDO19	2.85 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	300 mA	OFF
LDO20	2.85 V	1.5/1.8/2.4/2.5/2.6/2.7/2.85/3.0	300 mA	OFF

- Fault analysis and location

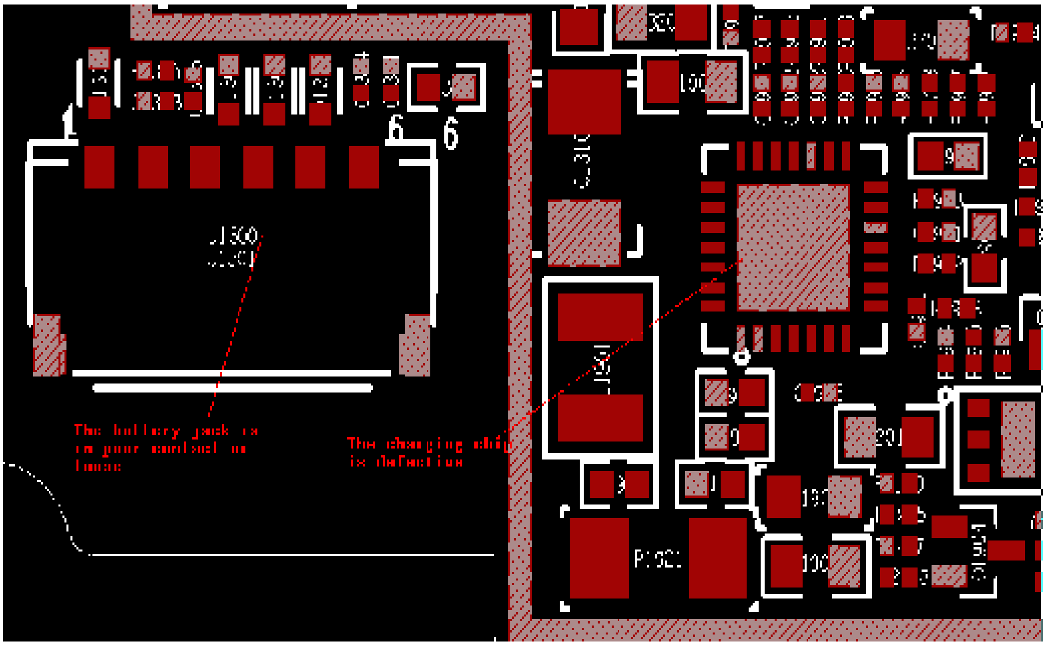
Table 4-2 lists the possible faults of the AP power circuit.

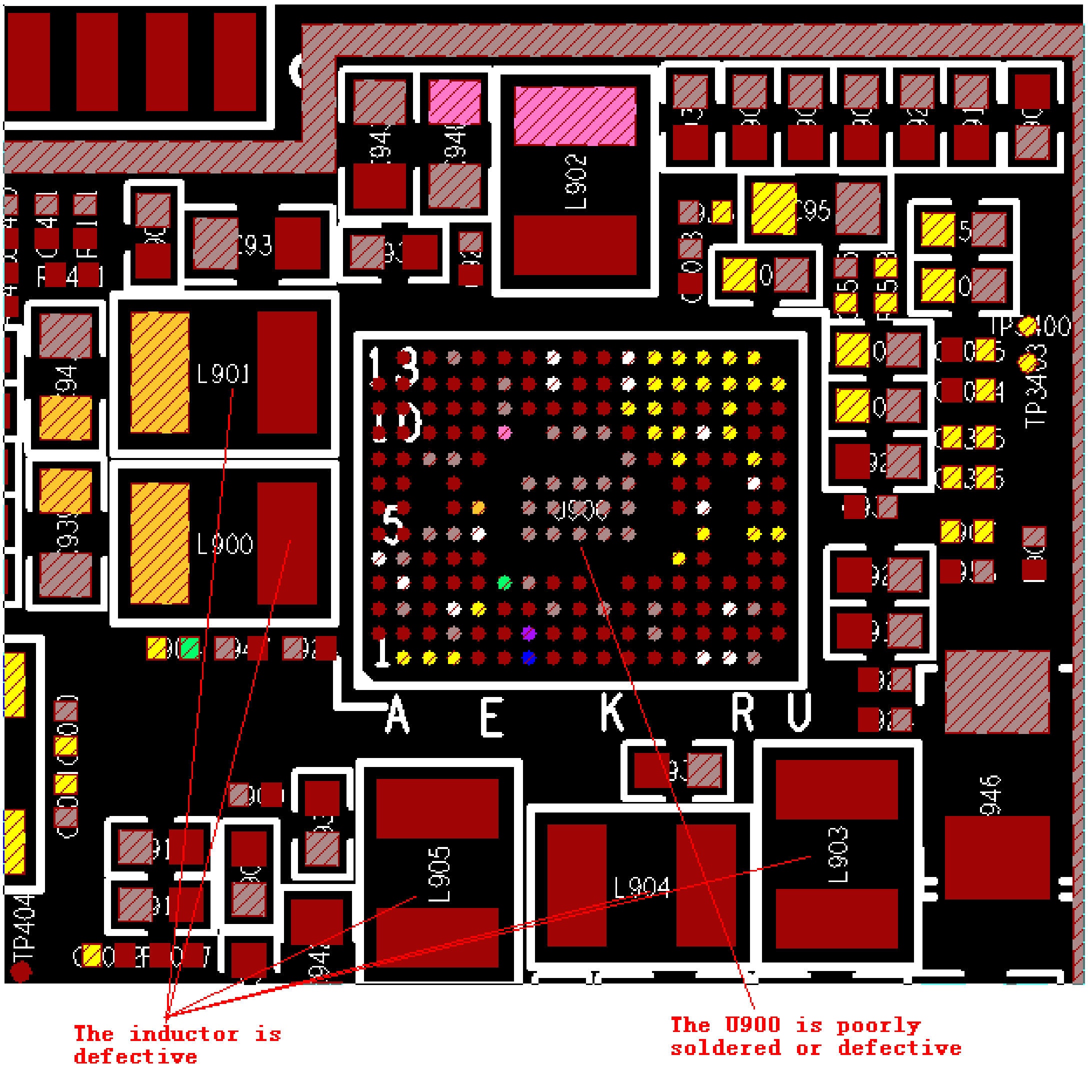
Table 4-2 Possible faults of the AP power circuit

No.	Symptom	Defect Position	Cause Analysis
1	The system cannot be powered on.	Flexible printed circuit (FPC)	• The FPC is disconnected. • The FPC and spring leaf are not in position. • The PMU is poorly soldered. • The charging chip is defective.

Figure 4-8 shows the possible faults of the AP power circuit.

Figure 4-8 Possible faults of the AP power circuit



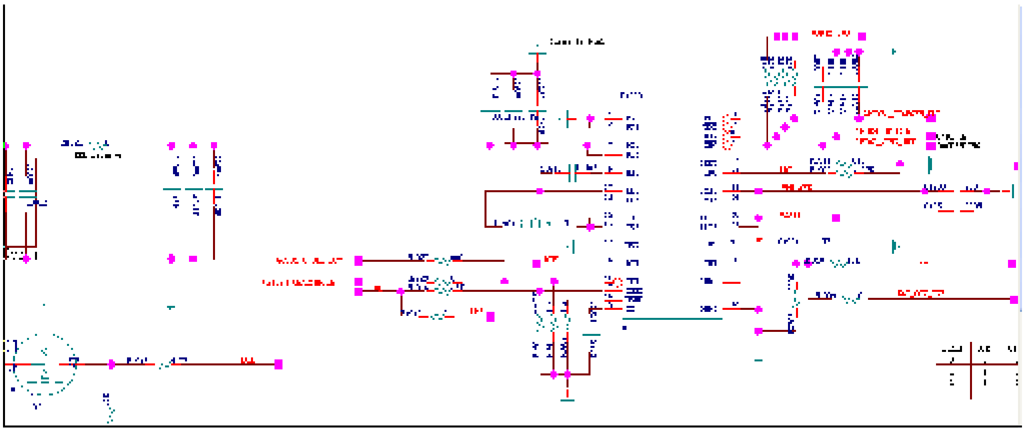


Working Principles of the AP Charging Circuit

- Working principles

Figure 4-9 shows the working principles of the AP charging circuit.

Figure 4-9 Working principles of the AP charging circuit



- Circuit analysis

  The S10 uses a dedicated charging management chip Max8903 to manage the charging process. The Max8903 chip needs only to determine whether to charge the battery. If the battery needs to be charged, the Max8903 chip is enabled; otherwise, the Max8903 chip is disabled. The Max8903 chip integrates a charging solution, which supports three charging states: trickle charging, constant-current charging, and pulse charging. The same charging circuit is used regardless of what charging mode is applied.

  If the signal level of the DCM is high, it indicates that the DC input current is restricted. The value 1 indicates that the DC input current is restricted by the IDC-to-ground resistance. The value 0 indicates that the DC input current is confined to 500 mA or 100 mA.

  CNE is used to enable or disable the charging current. It is Active-low.

  IUSB is used to restrict the input current of the USB peripheral inserted into the host.

  ISET is used to control the battery charging current. The maximum battery charging current is 2 A.

- Fault analysis and location

  Symptom: Two types of faults may occur on the charging circuit.

  - VPH_PWR does not output power. The MAX8903 is a charging chip in DC-DC mode. If it does not output power, probably the chip body or certain inductors are abnormal.
  - The battery cannot be charged. This fault is attributable to the following factors:

    (1) Software fault. If CEN is not active, the MAX8903 chip cannot start the charging mode.

    (2) Battery fault. The NTC resistance is abnormal.

    (3) The resistor mapping to the charging current of the IDC pin is abnormal.

- Circuit signals

Table 4-3 lists the signals of the AP charging circuit.

Table 4-3 Definitions of signals of the AP charging circuit

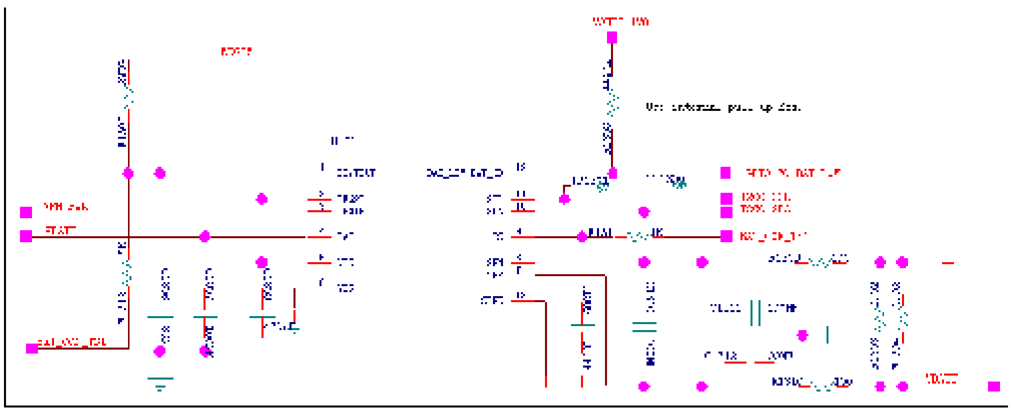
Signal Name	Function	Test Reference Value or Oscillogram
VCHG	Power input end of the charger Charger input detection	Detectable range: 0–6 V
DCM	Charging control mode	None
CEN	Charging current enabling signal, which is Active-low	
IUSB	A signal used to restrict the input current of the USB peripheral inserted into the host	
VPH_PWR	Primary power supply to the power module	Power voltage range: 0–4.2 V
ISET	A signal used to control the battery charging current (The maximum battery charging current is 2 A)	
V_BATT	Input end during battery voltage detection and output end during trickle charging The detection status does not change. Only the port is detected.	Power voltage range: 0–4.2 V

Working Principles of the Coulometer Circuit

- Working principles

Figure 4-10 shows the working principles of the coulometer circuit.

Figure 4-10 Working principles of the coulometer circuit



- Circuit analysis

The BQ27510 uses a technology called impedance tracking. An LDO is integrated to monitor the electric energy of the system battery and can be directly driven by the battery with fewer external circuits under any system voltage condition.

In addition to the simplified design and integration of battery monitoring, the system can exactly measure the remaining electric energy of each lithium ion battery, so that the battery endurance can be predicted even if the battery has aged. The precise battery energy measurement function helps the system to intelligently manage the remaining electric energy of the battery, notify users of the remaining system runtime, and prolong the system runtime as much as possible.

The mobile application processor just relies on precise battery data to better optimize the power system efficiency of mobile devices. The BQ27510 will precisely give an alert about the remaining electric energy of the battery to users, so that users can save data to non-volatile memory before the system is closed. This ensures that users' work is not lost before the electric energy of the battery is exhausted.

The BQ27510 circuit features simple design. The battery voltage and battery NTC are connected to circuit components, and IIC control is applied. In addition, differential current detection is implemented.

- Fault analysis and location

  Symptom: The remaining electric energy of the battery is low, causing the system to be powered off. Probably the data Flash of the BQ27510 is abnormal or IIC access fails.

  Solution: Replace related components.

- Circuit signals

Table 4-4 lists the signals of the coulometer circuit.

Table 4-4 Definitions of signals of the coulometer circuit

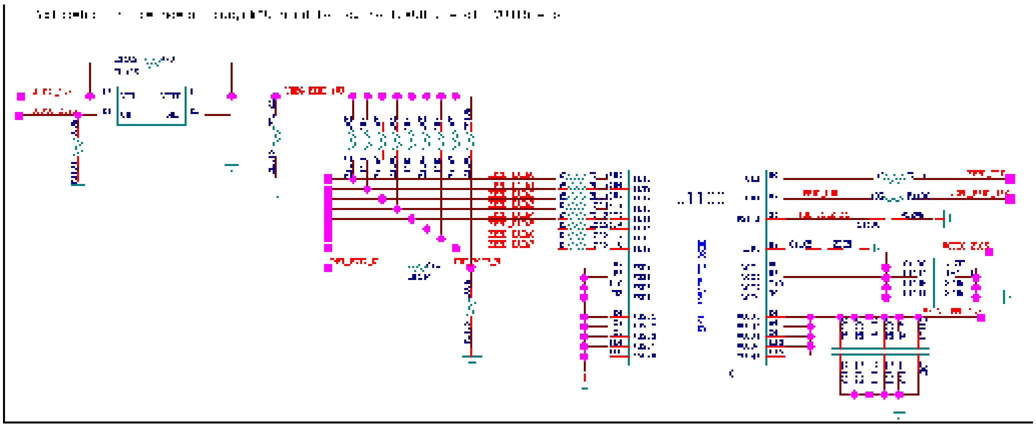
Signal Name	Function	Test Reference Value or Oscillogram
VPH_PWR	Primary power used to supply power to the internal LDO	Power voltage range: 0–4.2 V
BAT_CON_TS1	Battery NTC used to monitor the temperature of the battery	
V_BATT	Input end for battery voltage detection	Power voltage range: 0–4.2 V
I2C0_SCL	IIC interface	1.8 V
I2C0_SDA	IIC interface	1.8 V

Working Principles of the eMMC Circuit

- Working principles

Figure 4-11 shows the working principles of the eMMC circuit.

Figure 4-11 Working principles of the eMMC circuit



- Circuit analysis

  The circuit supports 8-bit SDIO interfaces.

  The I/O power pin VOUT5_1V8 and the power supply pin VOUT0_2V85 need to meet certain sequencing requirements.

  The reset signal PMU_RST2_N comes from the PMU. Its signal level is 2.6 V. This signal experiences voltage dividing by a resistor before it is sent to the eMMC.

- Fault analysis and location

  Symptom: The eMMC circuit seldom fails. Peripheral circuits, however, may have problems such as poor soldering and component defects. For example, the U1103 is a power-on sequencing control component and may fail in certain conditions.

- Circuit signals

Table 4-5 lists the signals of the eMMC circuit.

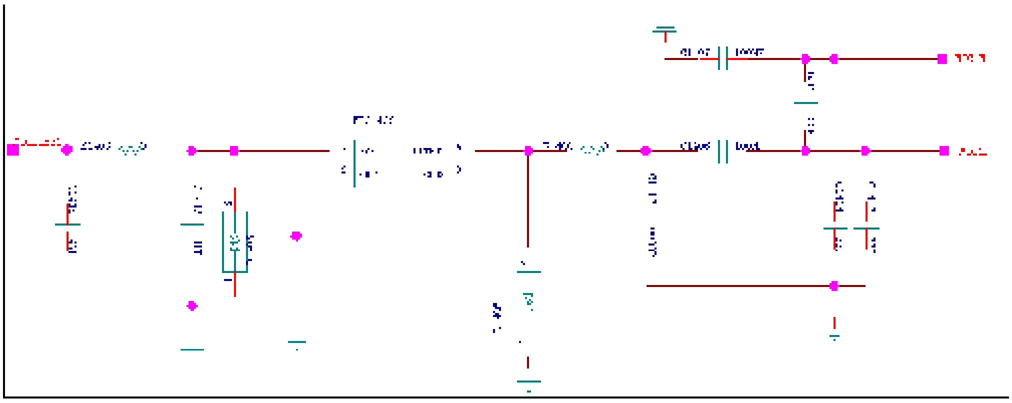
Table 4-5 Definitions of signals of the eMMC circuit

Signal Name	Function	Test Reference Value or Oscillogram
EMMC_DATA[0:7]	Data bus of the eMMC	
PMU_RST2_N1	Reset signal of the eMMC	
EMMC_CLK	Clock signal of the eMMC	
EMMC_CMD	Command signal of the eMMC	
VREG_EMMC_1V8	I/O power of the eMMC	
VOUT0_2V85	Internal working power supply of the eMMC	

Working Principles of the MIC Circuit

- Working principles

Figure 4-12 Working principles of the MIC circuit



- Circuit analysis

  The MIC used on the PCBA comes from Knowles. The MIC bias voltage provided by the PMU is input to the PMU after passing a single-ended-to-differential converter.

- Fault analysis and location

  Symptom: The MIC has a poor recording effect, or noise is heard.

  Solution: Replace the MIC, and then check whether the fault is cleared. If the fault persists, check whether the bias voltage is normal and whether the PMU U900 is faulty.

- Circuit signals

Table 4-6 lists the signals of the MIC circuit.

Table 4-6 Definitions of signals of the MIC circuit

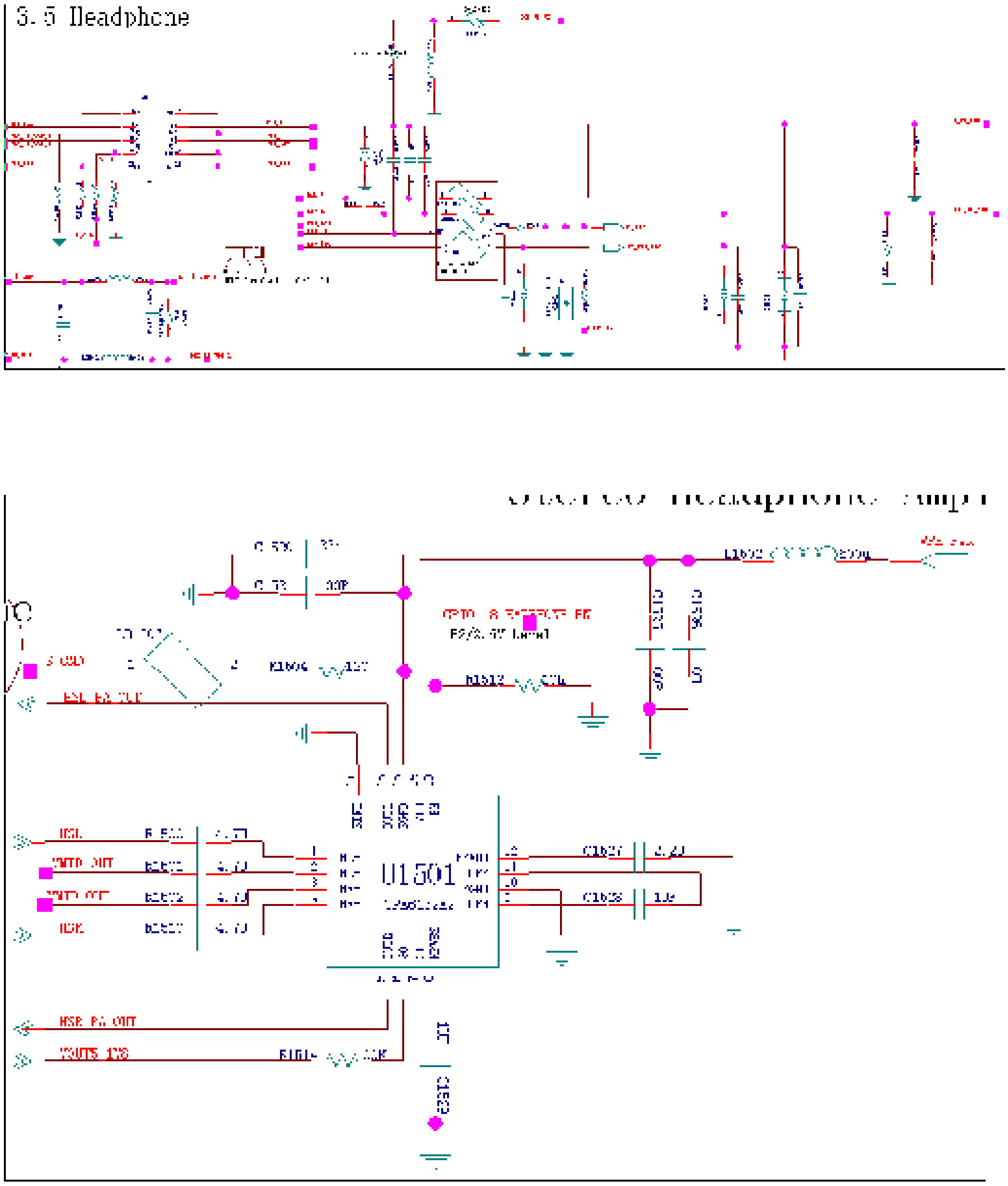
Signal Name	Function	Test Reference Value or Oscillogram
MICBIAS1	MIC bias voltage	
MIC1P	MIC differential signal	
MIC1N	MIC differential signal	

Working Principles of the Headset Circuit

- Working principles

Figure 4-13 shows the working principles of the headset circuit.

Figure 4-13 Working principles of the headset circuit



- Circuit analysis

  The PMU outputs headset signals to the headset power amplifier U1501. After being amplified by the U1501, the signals reach a small headset board through the FPC jack J1500.

  The power of the U1501 is supplied by the VPH_PWR pin. A step-up circuit is designed inside the U1501 to ensure that the output signals of the headset are not distorted under different voltage conditions. The signals output by the U1501 are sent to a BTB jack and then reach a small headset board through the FPC jack. Finally, the signals are output to the headset.

- Fault analysis and location

- The headset does not output signals. Check whether the small headset board is faulty, the FPC jack is properly connected, the BTB jack on the PCBA is normal, and the headset power amplifier U1501 is working properly.
- The headset MIC cannot record voice. Check the small headset board, the FPC jack, and the PMU in turn.

- Circuit signals

Table 4-7 lists the signals of the headset circuit.

Table 4-7 Definitions of signals of the headset circuit

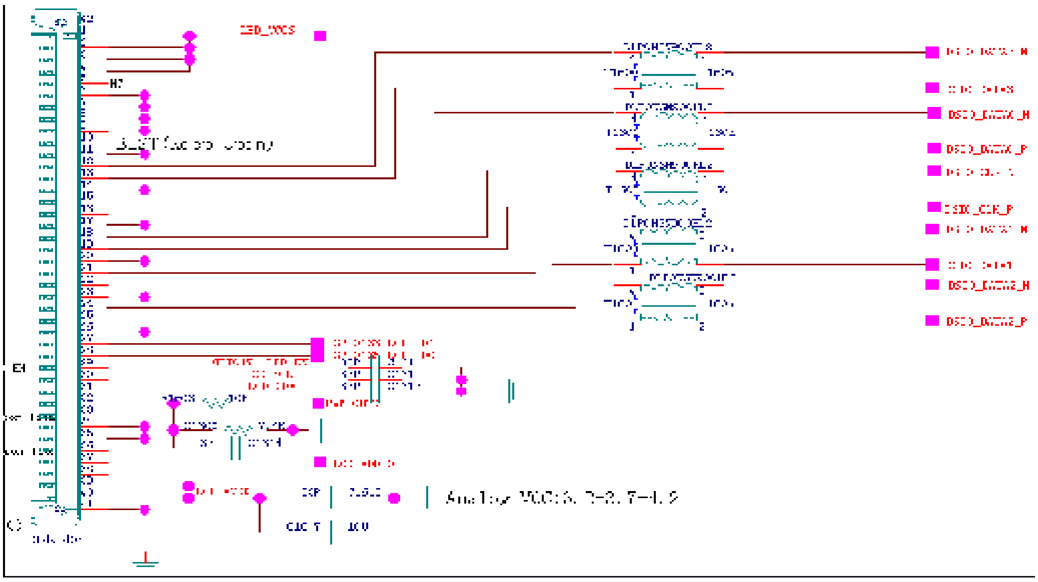
Signal Name	Function	Test Reference Value or Oscillogram
HSL/R_PA_OUT	Headset signal output by the headset power amplifier	
HSL/R	Headset signal output by the PMU	
VIMD_OUT	19.2°C temperature detection	
EAR_L/R	Signal output by the headset power amplifier to the headset jack	
EAR_DET	Headset detection	

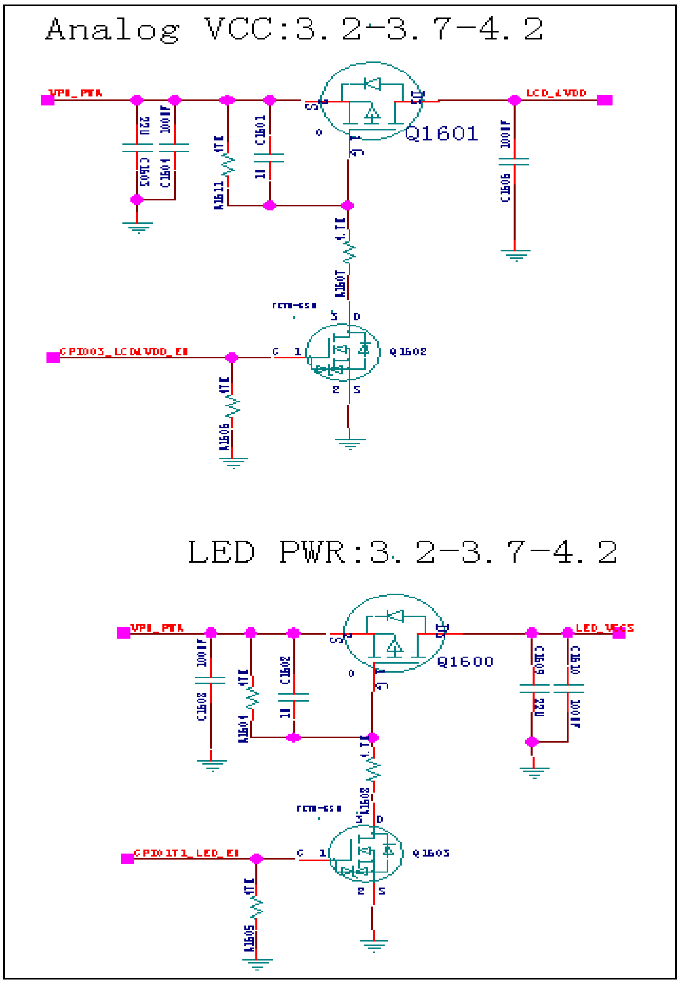
Working Principles of the LCD Circuit

- Working principles

Figure 4-14 shows the working principles of the LCD circuit.

Figure 4-14 Working principles of the LCD circuit





- Circuit analysis

  The LCD involves simple peripheral circuits. All drive circuits are integrated on a circuit board of the LCD.

  The power supply of the LCD circuit is simple and needs only to provide analog voltages and supply power to the LED.

  The data signals of the LCD circuit are the MIPI interface signal and five pairs of differential signals (one pair of clock signals and four pairs of data signals).

  The control signals of the LCD circuit are the IIC interface signal, backlight enabling signal, and PWM control signal.

- Fault analysis and location
  - Both the backlight LED and the LCD are off. Check whether the power circuit is normal, whether jacks are in good contact (Ensure that cables are properly plugged and unplugged), and whether the system has been properly started.
  - The LCD is off but the backlight LED is on. Check whether the power circuit is normal and whether jacks are in good contact (Ensure that cables are properly plugged and unplugged).
  - The LCD is flashing or garbled. Check whether the PWM is working properly and whether the materials of the LCD are normal.
- Circuit signals

Table 4-8 lists the signals of the LCD circuit.

Table 4-8 Definitions of signals of the LCD circuit

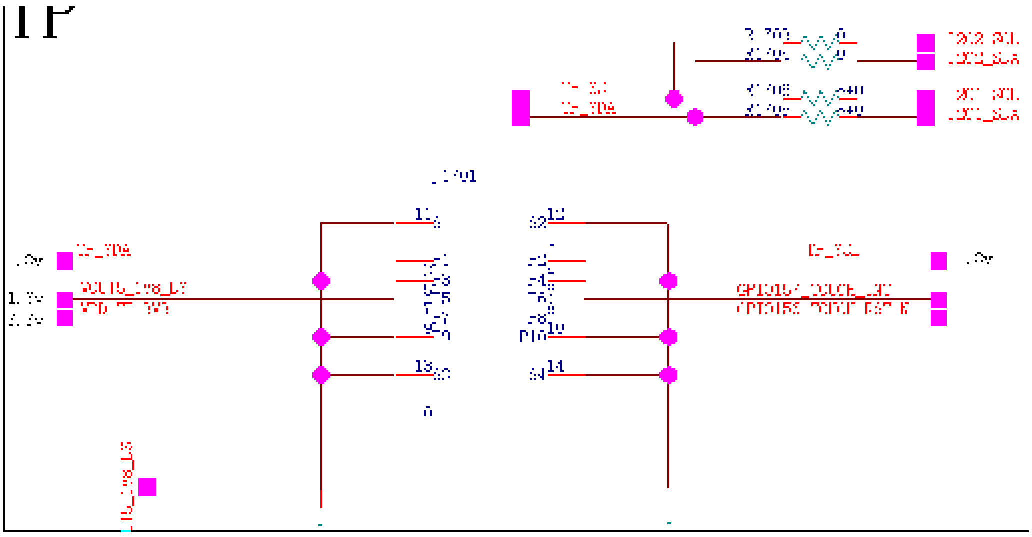
Signal Name	Function	Test Reference Value or Oscillogram
DSI0_DATA[3:0]_N/P	MIPI data	
DSI0_CLK_N/P	MIPI differential clock	
GPIO171_LED_EN	Backlight LED enabling	
LCD_SCL/SDA	IIC control signal of the LCD	
PWM_OUT0	Signal used by the AP to control the backlight LED of the LCD	
LCD_VDDIO	I/O power of the LCD	
LCD_AVDD	Analog voltage of the LCD	3.2–4.2 V
LED_VCCS	Power supply of the backlight LED	

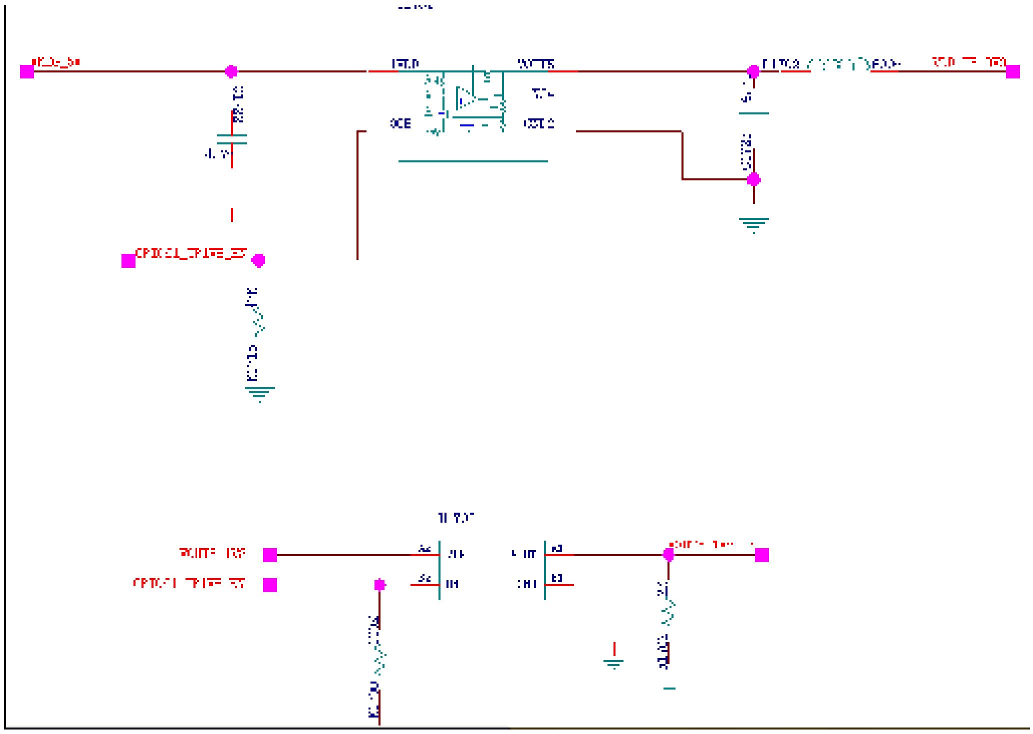
Working Principles of the TP Circuit

- Working principles

Figure 4-15 shows the working principles of the TP circuit.

Figure 4-15 Working principles of the TP circuit





- Circuit analysis

  The TP involves simple power interfaces. It has only two power channels, one of which is 3.3 V and the other is 1.8 V. The 3.3 V voltage is separately supplied to prevent system power ripples from affecting the usage effect of the TP. The 1.8 V voltage provides the I/O power. There is no power-on sequencing requirement for both voltages.

  The IIC interface is used for data transmission. Its signal level is 1.8 V.

- Fault analysis and location

  Symptom: The TP does not respond at all, or partially responds.

  Solution: Check whether the BTB jack is properly soldered and in good contact. Then check whether the two power channels normally supply power and whether the IIC buses are working properly.

- Circuit signals

Table 4-9 lists the signals of the TP circuit.

Table 4-9 Definitions of signals of the TP circuit

Signal Name	Function	Test Reference Value or Oscillogram
GPIO61_TP1V8_EN	1.8 V power switch of the TP	
TP_SCL	IIC of the TP	
TP_SDA	IIC of the TP	

Working Principles of the Camera Circuit

- Working principles

Figure 4-16 shows the working principles of the rear camera.

Figure 4-16 Working principles of the rear camera

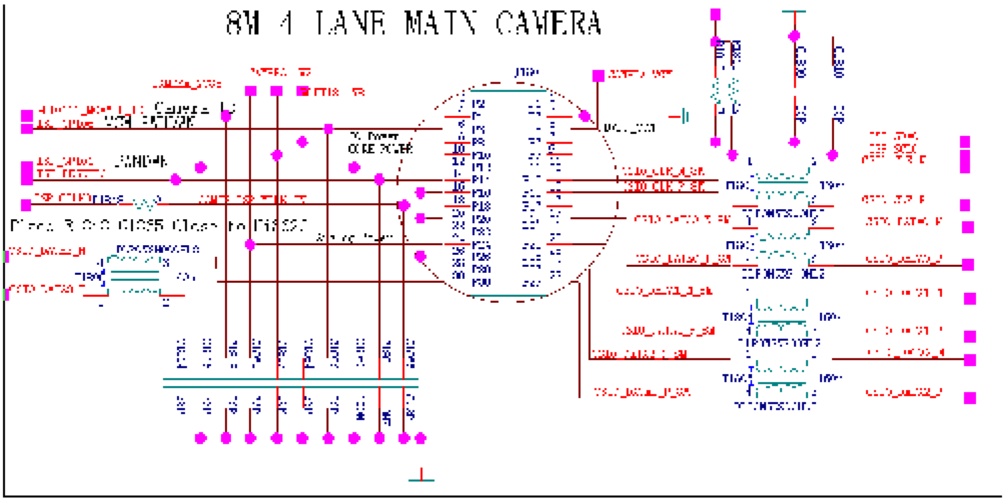
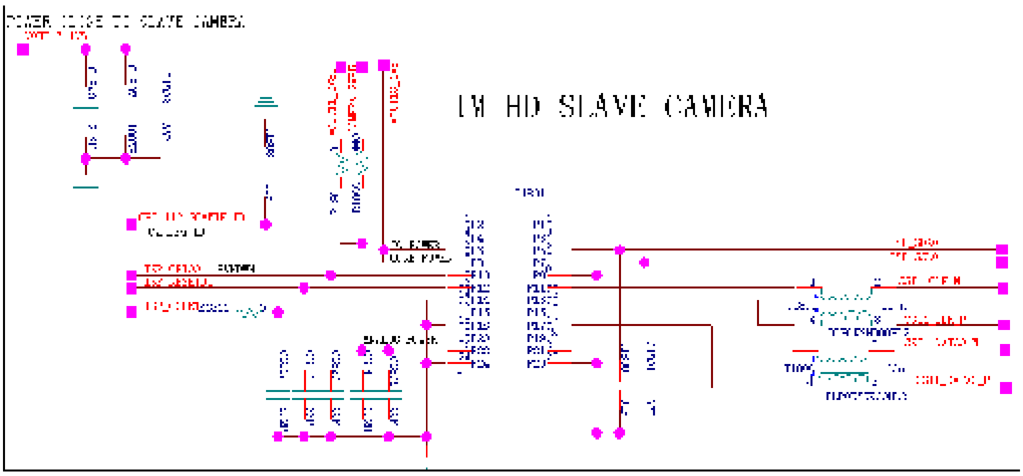


Figure 4-17 shows the working principles of the front camera.

Figure 4-17 Working principles of the front camera



- Circuit analysis

  The camera circuit uses MIPI interfaces. Five pairs of MIPI buses (four pairs of data buses and one pair of clock buses) are designed for the rear camera, and two pairs of MIPI buses (one pair of data buses and one pair of clock buses) for the front camera.

  The signal level of the data transmission interfaces is 1.8 V.

- Fault analysis and location

  Symptom: The camera does not display any information.

Solution: Check whether the BTB jack is properly soldered and in good contact. Then check whether the power supply is normal and whether the IIC buses are working properly.

- Circuit signals

Table 4-10 lists the signals of the camera circuit.

Table 4-10 Definitions of signals of the camera circuit

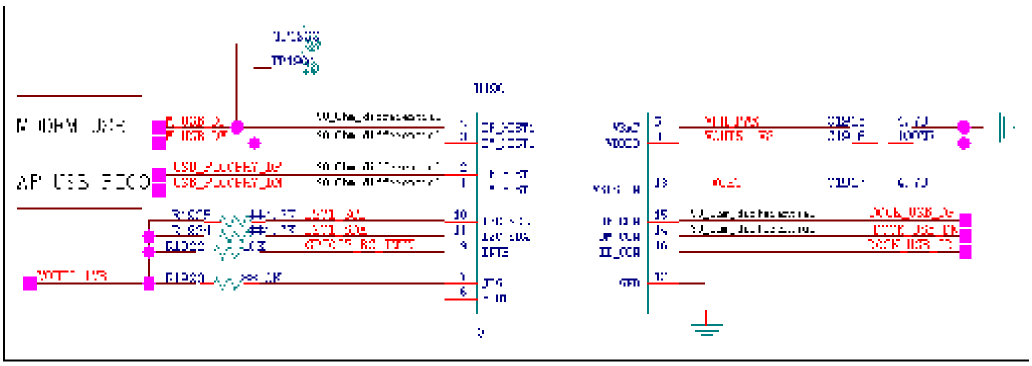
Signal Name	Function	Test Reference Value or Oscillogram
CSI0_DATA[0:3]_N/P	Data bus of the rear camera	
CSI0_CLK_P/N	Differential MIPI clock signal pair for the rear camera	
CSI1_DATA0_N/P	Data bus of the front camera	
CSI1_CLK_P/N	Differential MIPI clock signal pair for the front camera	

Working Principles of the BC1.1 Circuit

- Working principles

Figure 4-18 shows the Working principles of the BC1.1 circuit.

Figure 4-18 Working principles of the BC1.1 circuit



- Circuit analysis

  In fact, the BC1.1 chip is an analog switch. It uses a pair of USB buses as external interfaces and uses two USB buses as input interfaces. One USB bus is connected to a USB PHY controller on the AP side, and the other USB bus is connected to a USB controller on the modem side to implement the debugging function. By default, the USB PHY controller on the AP side maintains connectivity with external devices.

  When an external USB peripheral is connected, the BC1.1 chip detects the external USB peripheral and reports a message to the AP, so that the AP initiates a protocol link to the USB peripheral. Another function of the BC1.1 chip is to identify a USB peripheral by detecting the ID pin of the USB peripheral, so that the charging current of the charging chip can be properly controlled to 500 mA, 1.5 A, or 2 A.

The BC1.1 chip communicates with the AP through IIC and USB interfaces. The signal level of the IIC interface is 1.8 V. The IIC interface enables the AP to read and configure status information about the BC1.1 chip. The USB interface is used for data communication.

- Fault analysis and location

  Symptom: The BC1.1 chip cannot detect a USB peripheral.

  Solution: Check whether the BC1.1 chip is properly soldered and whether its coaxial cable or FPC cable is in good contact.

- Circuit signals

Table 4-11 lists the signals of the BC1.1 circuit.

Table 4-11 Definitions of signals of the BC1.1 circuit

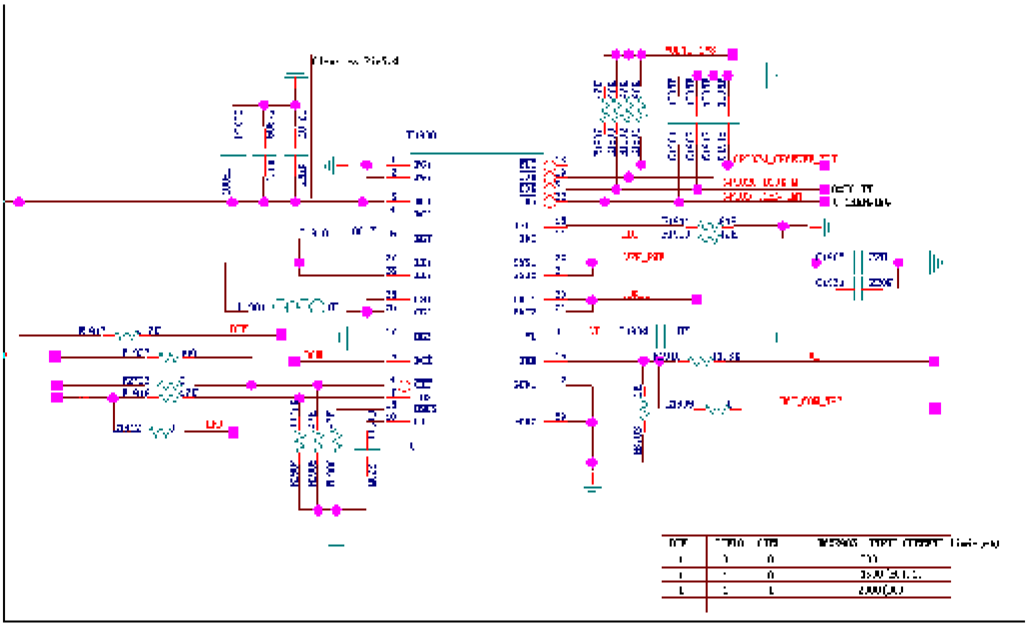
Signal Name	Function	Test Reference Value or Oscillogram
USB_PICOPHY_DP/N	USB bus on the AP side	
M_USB_DP/N	USB bus on the modem side	
I2C1_SCL/SDA	IIC bus 1	
GPIO27_BC_INTN	Terminal signal reported by the BC1.1 chip to the AP	
DOCK_USB_DP/N	Output USB bus	
DOCK_USB_ID	USB ID signal	

Working Principles of the Charging Circuit

- Working principles

Figure 4-19 shows the working principles of the charging circuit.

Figure 4-19 Working principles of the charging circuit

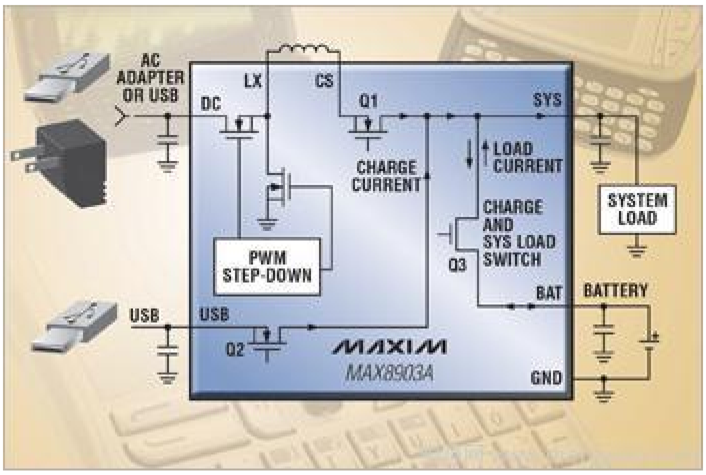


- Circuit analysis

  The MAX8903A uses the switch mode of the Smart Power Selector™ circuit and a DC-DC charger. The charger has a high switching frequency which is typically 4 MHz. In addition, the MAX8903A contains loads for power switching between the battery and external power supply, power switches required to charge the loads, and a current detection circuit. The MAX8903A has optimized each chargeable lithium-ion battery.

Figure 4-20 shows the working principles of the MAX8903A.

Figure 4-20 Working principles of the MAX8903A



The MAX8903A can use two independent input ports or only one input port to receive power supply from a USB peripheral and an AC adapter. When external power supply is connected, the Smart Power Selector circuit allows the system to operate without any battery or operate with a battery in deep discharge mode. The Smart Power Selector circuit can automatically switch the system power supply form the battery to external power supply to make full use of the finite power supply capability of the USB peripheral or the AC adapter, so that the battery is charged at the same time when the power supply of the system is guaranteed.

The DC input voltage range of the converter is 4.1 V to 16 V. A USB peripheral, AC adapter, or car charger can be directly used to charge the battery. If a dedicated USB peripheral is used, its input voltage can range from 4.1 V to 6.6 V. The DC input current is restricted and can reach a maximum of 2 A. Both the DC power and the USB power support three input modes: 100 mA, 500 mA, and USB suspension. The maximum charging current can be adjusted to 2 A to support a wide range of battery capacity.

The MAX8903A also provides other functions, such as thermal adjustment, over-voltage protection, power output in charging or faulty state, power-good detection, battery thermistor detection, and a charging timer.

- Fault analysis and location

  Symptom: Charging fails, and no power is supplied to the system.

  Solution: Check whether the MAX8903 is working properly.

- Circuit signals

Table 4-12 lists the signals of the charging circuit.

Table 4-12 Definitions of signals of the charging circuit

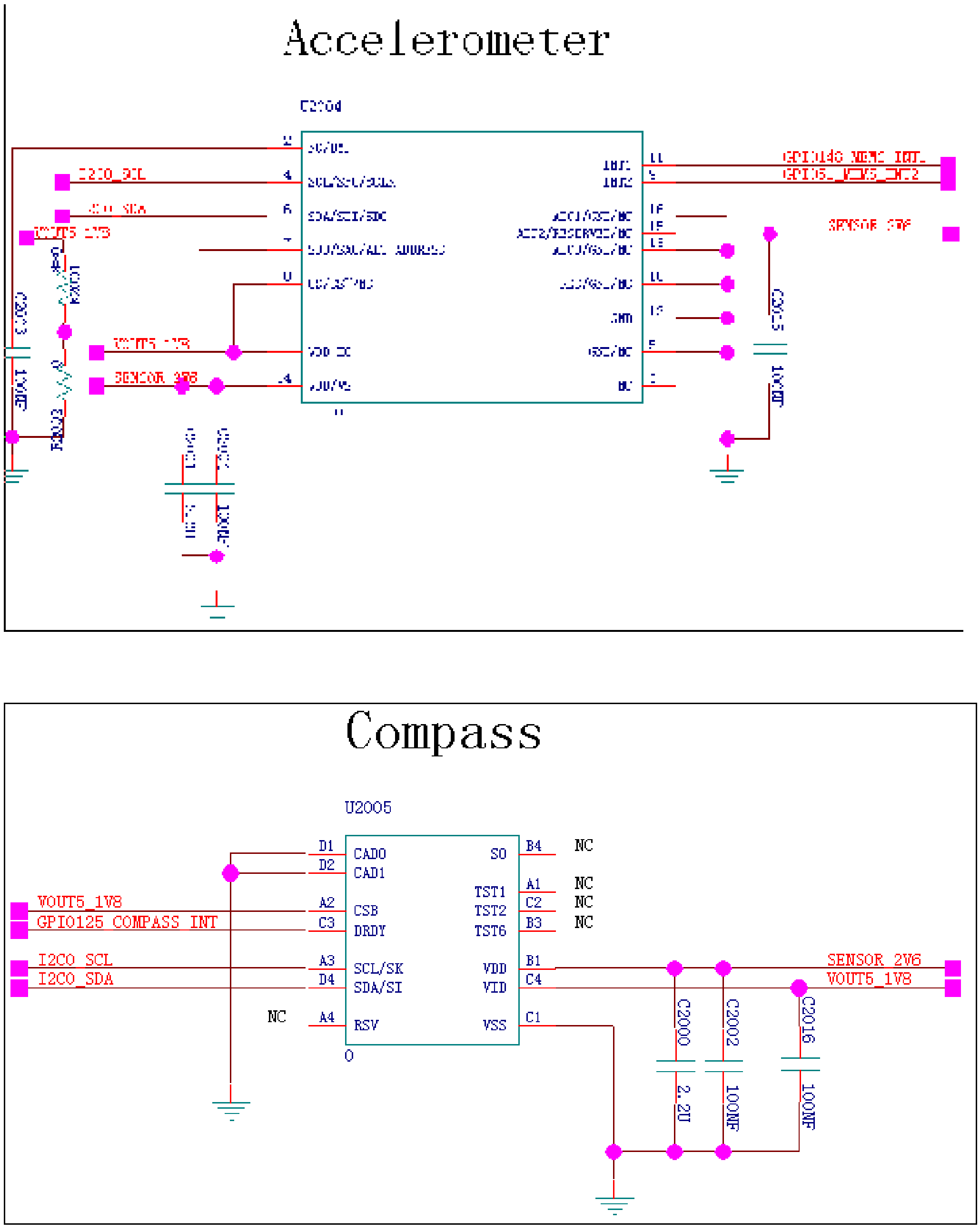
Signal Name	Function	Test Reference Value or Oscillogram
VCHG	Total power input	
GPIO74_CHARGER_EN	Charging enabling pin	
VPH_PWR	Power output by the charging chip to succeeding systems	
GPIO20_DCOK_N	DC insertion indication	
GPIO24_CHARGER_FLT	Charging status indication	
GPIO5_VCHG_INT	Charging interruption indication	
VBATT	Battery power	
GPIO22_ISET_CTRL0/1	Charging current control	

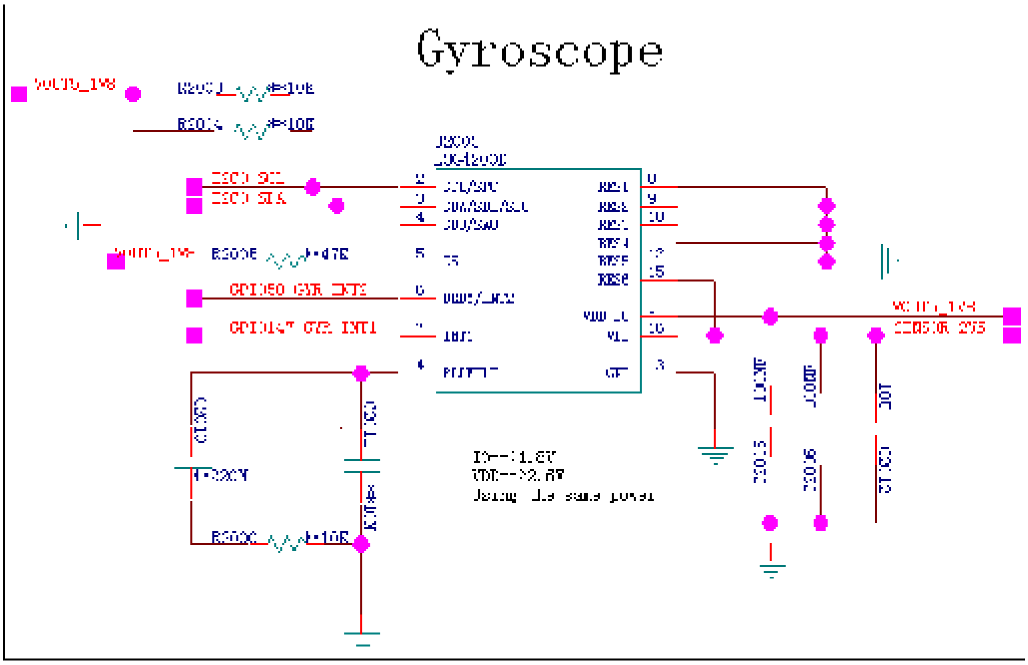
Working Principles of the Sensor Circuits

- Working principles

Figure 4-21 shows the working principles of the sensor circuits.

Figure 4-21 Working principles of the sensor circuits





- Circuit analysis

  Sensors use IIC interfaces for communication. Their power supply is simple. The working voltage is 2.6 V, and the I/O voltage is 1.8 V.

- Fault analysis and location

  Symptom: The sensors do not respond.

  Solution: Check whether the power supply of the sensors is normal and whether the IIC interfaces provide normal communication.

- Circuit signals

Table 4-13 lists the signals of the sensor circuit.

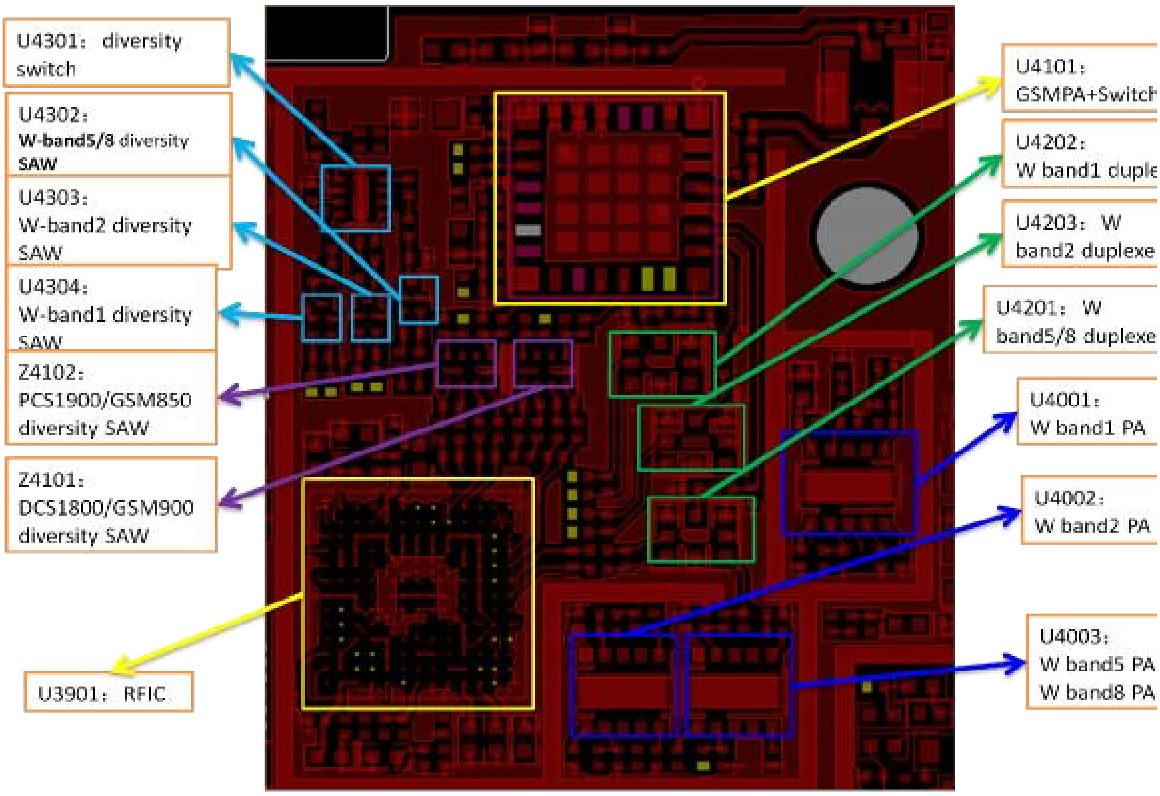
Table 4-13 Definitions of signals of the sensor circuit

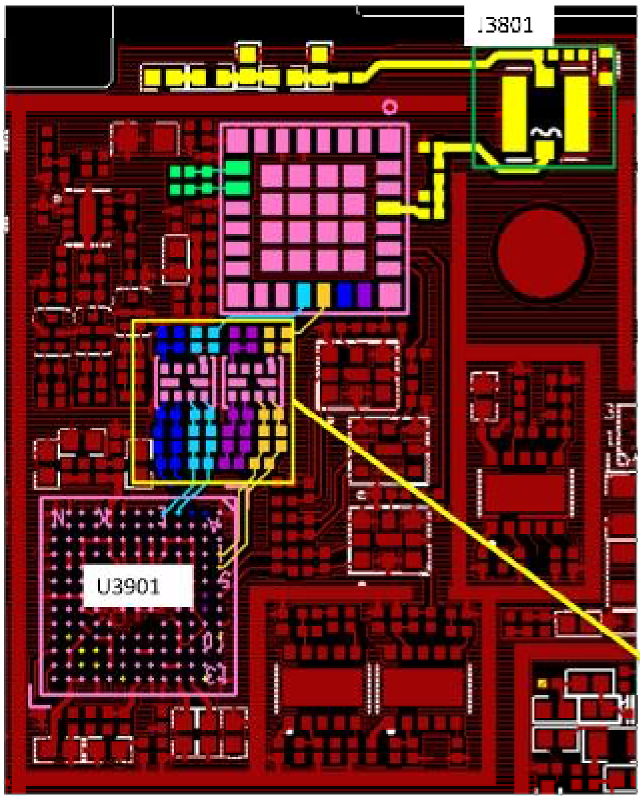
Signal Name	Function	Test Reference Value or Oscillogram
IIC0_SDA/SCL	IIC bus	
SENSOR_2V6	Working power of sensors	

4.4 Circuit Analysis and Troubleshooting for the Modem Unit

Figure 4-22 shows the circuits of the modem unit.

Figure 4-22 Circuits of the modem unit



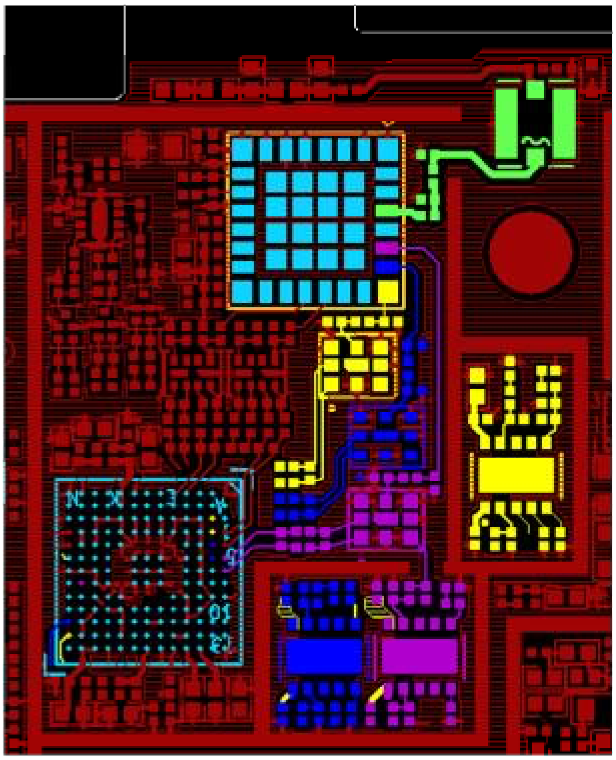


Transmit: The two green channels are transmit signals of the low-band GSM850/GSM900 and high-band DCS1800/PCS1900. They reach the RF connector 3801 after passing the GSM PA and the antenna switch U4101. The yellow parts indicate components on the channels of signals output by the antenna switch.

Receive: Signals reach the antenna switch U4101 from the J3801, pass the SAW Z4101 and Z4102, and then reach the U3901.

The channels indicated here are the receive channels of the GSM850, PCS1900, GSM900, and DCS1800 from left to right.

WCDMA Channels

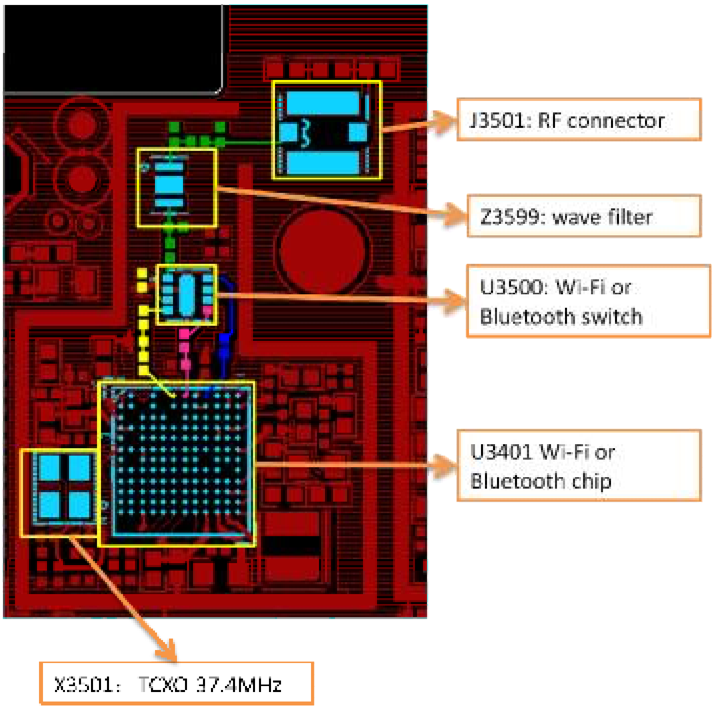


1. Yellow indicates RF channels of WCDMA band 1.
2. Pink indicates RF channels of WCDMA band 5/8.
3. Blue indicates RF channels of WCDMA band 2.

Transmit: Transmit signals from the U3901 reach the PAs of respective WCDMA bands through a matching circuit, then enter the duplexers of respective WCDMA bands, and finally reach the RF connector J3801 after passing the antenna switch U4101.

Receive: Receive signals from the J3801 reach the duplexers of respective WCDMA bands after passing the antenna switch U4101, and then reach the U4101 through a receive matching circuit.

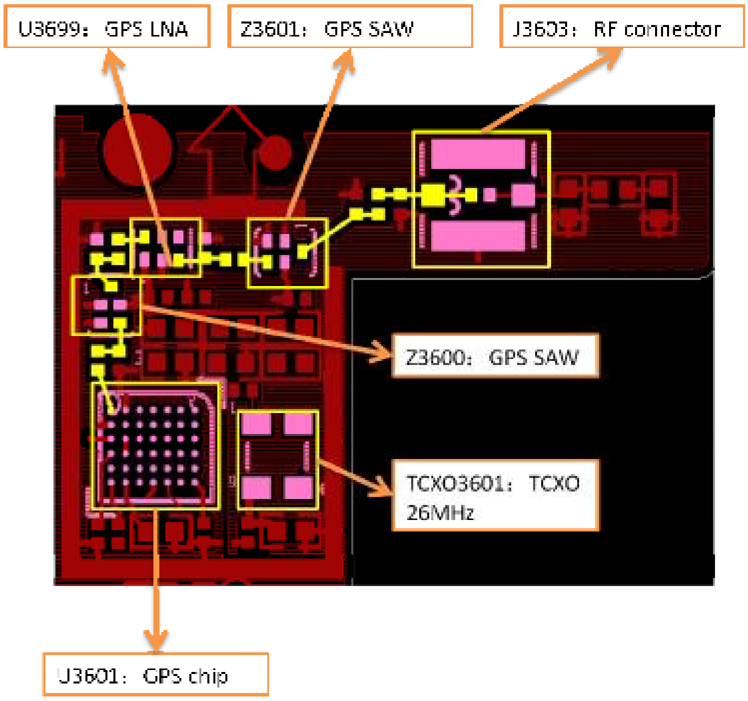
Wi-Fi / Bluetooth Channels



Yellow indicates Wi-Fi transmit channels.
Blue indicates Bluetooth transmit channels.
Pink indicates Wi-Fi or Bluetooth receive channels.
Green indicates common channels before switches.

Wi-Fi or Bluetooth transmit signals are sent from the U3401 to the switch U3500, pass an SAW filter, and then reach the RF connector J3501.
Wi-Fi or Bluetooth receive signals enter from the RF connector J3501, reach the SAW filter, pass the switch U3500, and then reach the U3401.

GPS Channels



Yellow indicates GPS receive channels。
GPS signals arrive at the GPS SAW filter Z3601 from the RF connector J3603. Then the signals are amplified by the LNA U3699, pass the GPS SAW filter Z3600, and finally reach the GPS chip.

General Maintenance Process

Defect analysis

1. Surface mounting technology (SMT) defects account for a large proportion of board defects. Therefore, perform X-ray inspection and visually check defective boards before performing maintenance. Check associated components, such as inductors and capacitors, in addition to key chip components. For example, check whether dry solder joints exist, whether components are damaged, and whether defective materials are applied. After confirming that the components are normal, proceed to the following maintenance process.
2. If communication problems exist on boards or USB ports are unstable, analyze CT logs to determine whether the software or hardware is faulty.
3. To determine whether materials are defective, compare them with qualified board materials. Ensure that the materials are properly soldered. If materials are indeed defective, collect, isolate, and hand over the defective materials to TQC for quality inspection.
4. If materials need to be replaced for a board, apply the rework process to avoid procedural errors.

Common Faults of the CT Module

- AFC calibration failure

- WCDMA transmit links are faulty.
- The crystal oscillator is faulty.

- WCDMA TRX calibration failure
  - Check whether the WCDMA transmit power is normal. In most cases, soldering errors may exist on transmit links.
  - Check whether the PD link is normal.
  - Check whether the RX link is normal.
  - Check whether the DRX link is normal.
- GSM or EDGE TX calibration failure
  - Check whether the GSM PA is properly soldered.
  - Check whether the power supply and the control unit of the GSM PA are normal.
- Software version access failure or port enabling failure

Send the module to software or hardware engineers for processing.

Common Faults of the Bluetooth Module

- WCDMA inloop failure
  - Test the CT and Bluetooth again by using the same production test equipment, and then check whether the test result is normal.
  - If the fault persists, replace the PA of the respective frequency band and test the CT and Bluetooth again.
- WCDMA and GSM sensitivity test failure
  - Check whether environmental interference exists because the shielding box is uncovered or shielding measures are not taken.
  - Check whether SMT defects exist on receive links.
- Software version access failure or port enabling failure
  - Send the module to software or hardware engineers for processing.

Common Faults of the Wi-Fi Module

- Serious packet loss in the receive direction
  - Check whether environmental interference exists.
  - Check whether SMT defects exist on receive links.
  - Check whether SMT defects exist on the Wi-Fi chip.
  - Check whether the Wi-Fi chip is faulty.
- Small transmit power or poor EVM
  - Check whether the production test equipment is improperly calibrated, whether line loss is correct, and whether the voltage standing wave ratio (VSWR) and impedance of the test environment meet related requirements.
  - Check whether fixtures are fastened and thimbles are in good contact. Thimbles may be defective as they are used time and again.
  - Check whether SMT defects exist on transmit links.
  - Check whether SMT defects exist on the Wi-Fi chip.
  - Check whether the Wi-Fi chip is faulty.
- Software version access failure or port enabling failure

- Send the module to software or hardware engineers for processing.

Common Faults of the GPS Module

1. Check whether the production test equipment is properly calibrated.
2. Check whether the antenna is poorly soldered or defective.
3. Check whether SMT defects exist on the GPS receive link.
4. Check whether SMT defects exist on the GPS chip.
5. Check whether the GPS chip is defective.
6. Check whether ports cannot be enabled. If yes, send the module to software or hardware engineers for processing.

5 Software Upgrade

5.1 Upgrade Preparation

Table 5-1 lists the items to be prepared before upgrade.

Table 5-1 Upgrade preparation

Item	Description	Remarks
Upgrade file	The actual upgrade file takes precedence.	Upgrade by using a USB peripheral
Upgrade method	Upgrade by using a USB peripheral or a microSD card	
Tools	Download tool	
	Lithium-ion battery	Ensure that two bars or more battery power is remained.
	USB cable	
	PC	

5.2 Upgrading the Software by Using a USB Peripheral

5.2.1 Upgrading the Software by Using a microSD Card

You can upgrade the software by using a microSD card.

Copying the Upgrade Package

1. Check the current upgrade environment.

   Ensure that the microSD card is intact and can be read and written.

2. Obtain the upgrade package.

   Copy the **dload** directory to the microSD card.

Starting the Upgrade

1. Copy the **dload** directory to the root directory on the microSD card, and check whether the microSD card is damaged.
2. Confirm that the tablet is powered off.
3. Install the microSD card in the microSD card slot.
4. Power on the tablet. The system automatically upgrades its software from the microSD card.
5. After the upgrade is complete, the system automatically upgrades firmware. Remove the microSD card and restart the system after the firmware is upgraded.

Exception Handling

- Error 1

  A message is displayed on the screen during the upgrade, indicating that the upgrade failed. In this case, check whether improper operations are performed. Then remove the microSD card and install it again, or replace the microSD card and try upgrading the software again.

- Error 2

  If a failure occurs at the very beginning of the upgrade process, check whether the upgrade version is correct and whether the tablet or microSD card is damaged.

6 Disassembly Procedure

6.1 Tools

Screwdriver, straight tweezers, and plastic removers

6.2 Disassembly Preparation

Wear an ESD wrist strap and antistatic clothing. Do not leave any dirt such as fingerprints on the LCD screen or the lens of the LCD screen.

6.3 Disassembly Procedure

Disassembling the S10

Disassembling the Decorative Cover

6.4 Other Precautions

Before Disassembly

Wear an ESD wrist strap and antistatic clothing, and prepare tools.

During Disassembly

Disassemble the product carefully by using dedicated removers. Avoid any damage to the housing, PCBA components, or solder wires.

During Assembly

Assemble the product strictly in accordance with installation steps. Check whether operations have been correctly performed in the previous step after performing each step.

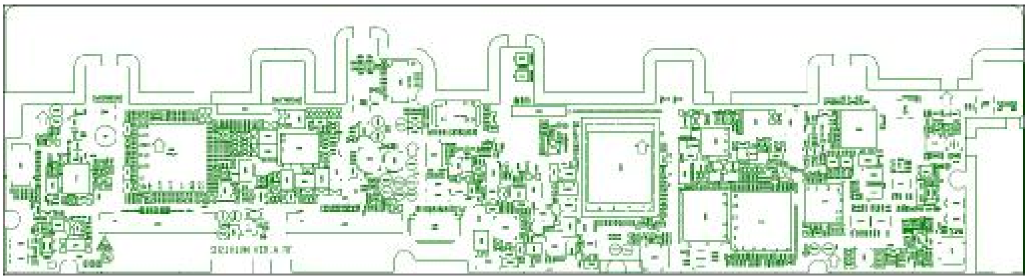
7 Appendix

7.1 PCBA Layout

PCBA Layout at the Top Layer

Figure 7-1 shows the PCBA layout at the top layer.

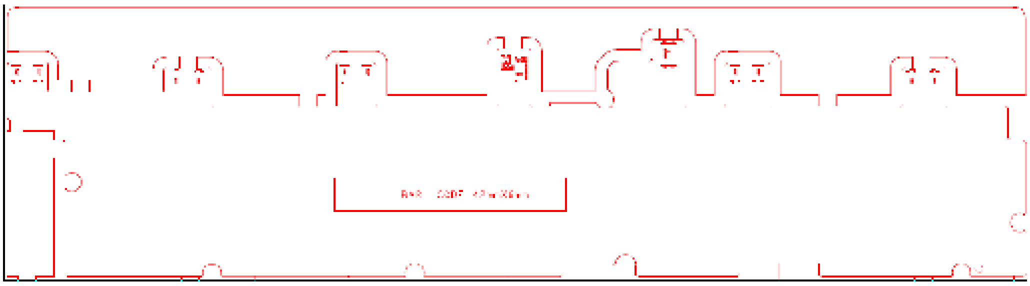
Figure 7-1 PCBA layout at the top layer



PCBA Layout at the Bottom Layer

Figure 7-2 shows the PCBA layout at the bottom layer.

Figure 7-2 PCBA layout at the bottom layer



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7.2 Test Spot List

Table 7-1 lists the test spots.

Table 7-1 Test spot list

Test Spot	Name	Description	Reference

7.3 Acronyms and Abbreviations

Abbreviation	Full Spelling
CDMA	Code Division Multiple Access
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LNA	Low Noise Amplifier
PM	Power Management
FSTN	Film Super Twisted Nematic
TCXO	Temperature-compensated crystal oscillator
ADC	Analog-to-Digital Converter
BPF	Band Pass Filter
UVLO	Under-Voltage Lockout
VCO	Voltage Controlled Oscillator
SBI	Serial Bus Interface